ELECTRONICS DESIGN FOR HIGH DENSITY CMUT ARRAY BASED ULTRASOUND IMAGING SYSTEM

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ELECTRONICS DESIGN FOR HIGH DENSITY CMUT ARRAY BASED ULTRASOUND IMAGING SYSTEM

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Honesty is the first chapter in the book of wisdom

Thomas Jefferson

In the loving memory of my mother Jahan Zeb Rashid

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SUMMARY

In catheter based ultrasound imaging applications, gathering real-time imaging data from a large number of transducer array elements is extremely challenging with the standard interconnect and transducer technology as there is a restriction on cable count due to the diameter of the catheter. Intracardiac Echocardiography (ICE) imaging systems require many cables connecting the transducer array elements at the tip of the catheter to the backend imaging systems. Reducing the number of cables using highly integrated front-end electronics, is essential for 3-D ICE imaging systems with 2-D imaging arrays. Cable reduction would also reduce the cost of the current 2-D imaging ICE catheters with 1-D imaging arrays and can enable to ICE imaging under MRI by reducing the RF induced heating of the catheters. Current approaches to cable reduction tend to rely on area and power-hungry circuits to function, making them unsuitable for use in catheters. This research explores the design of the CMOS receiver circuitry which implements a Time Division Multiplexing (TDM) scheme to address the receive cable restrictions of the catheter. This approach, implemented in the form of a direct digital demultiplexing technique, allows for a reduction in the number of analog signal processing stages required. Receive multiplexing alone is not enough to reduce the cable count since the same elements in the arrays are used as transmitters. Therefore, the CMOS circuitry should integrate transmit beamforming as well. For this purpose, this study also explores an on-chip programmable transmit beamformer circuit for producing focused and steered transmit beams. In this thesis, a system which uses an efficient real-time programmable on-chip transmit beamformer circuitry to reduce the cable count on the transmit side and analog 8:1 Time Division Multiplexing with Direct Digital Demodulation to reduce the cable count on the receive side is described and initial imaging results are presented.

CHAPTER 1
INTRODUCTION AND BACKGROUND

1.1 A Brief History of Medical Ultrasound Imaging

In 1794 Italian biologist Lazzaro Spallanzani first conducted extensive experiments on how bats navigate in complete darkness and started the research in ultrasound engineering [1]. Discovery of the piezoelectric effect by Pierre and Jacques Curie in March of 1880 was an important milestone in developing ultrasound technology [2]. After the tragic sinking of the RMS Titanic in 1912, and to detect submarines during First World War, the development of acoustic detection technology was highly demanded. In early 1917 French physicist Paul Langevin was the first scientist to send acoustic waves underwater successfully [3]. And in 1918 Langevin filed a patent [4] which lead to the discovery of SONAR (Sound Navigation and Ranging) system to detect underwater submarines. In 1942 Neurologist Karl Dussik published theoretical analysis of how ultrasound can be used to image body tissue [5]. Later in 1946 Dussik was the first who used ultrasound to diagnose a brain tumor. The first real-time ultrasound B-scanner was developed by Siemens Medical Systems of Germany in 1965. In the last fifty years, medical ultrasound continued to grow and mature. More details of the history of medical ultrasound transducers and imaging systems can be found in [6, 7]. Ultrasound is now used extensively by physicians for evaluating the heart, blood vessels, pelvic and abdominal organs [8]. Currently piezoelectric materials are predominantly used in the medical ultrasound imaging systems on the market. In 1990's Dr. Khuri-Yakub group at Stanford University demonstrated electrostatic based ultrasound transducers called Capacitive Micromachined Ultrasonic Transducers CMUTs [9, 10]. Because they have a wide bandwidth and can be easily integrated

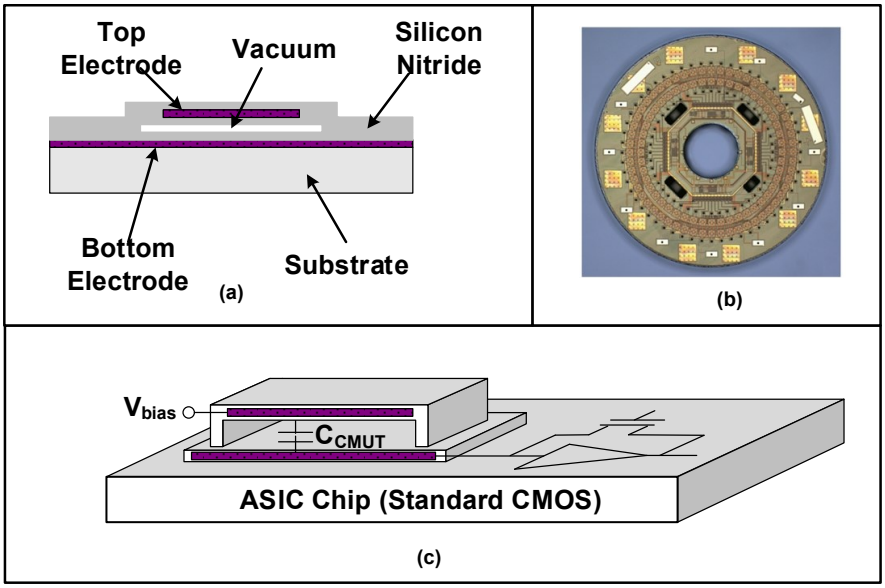

Figure 1.1: (a) Cross-sectional view of CMUT (b) Photo of a forward looking CMUT-on-CMOS based IVUS chip [13] (c) CMUT-on-CMOS schematic.

with electronics, CMUTs appear as a promising alternative for medical ultrasound transducers. Consequently, in recent years commercial CMUT imaging arrays have been developed. For example, in 2015 Kolo Medical, a San Jose, CA based startup company, demonstrated a 15 MHz 256-element linear array CMUT based commercial hand-held ultrasound probe at [11]. The CMUT probe can be used with Verasonics Vantage 128 Research Ultrasound system for medical imaging. This CMUT based system claims to have superior acoustic and imaging performance than its PZT counterpart. More recently, Hitachi from Japan announced new diagnostic ultrasound platform using CMUT based probes [12]. The capability of combining CMUTs and CMOS electronics on the same silicon substrate, CMUT-on-CMOS approach, has also been demonstrated recently. An example of this approach for forward looking intravascular ultrasound (IVUS) catheter has been demonstrated in [13]. Figure 1.1 shows implementation of CMUT-on-CMOS for IVUS catheter.

In a typical ultrasound imaging system, a 1-D piezoelectric array is used. Piezo-

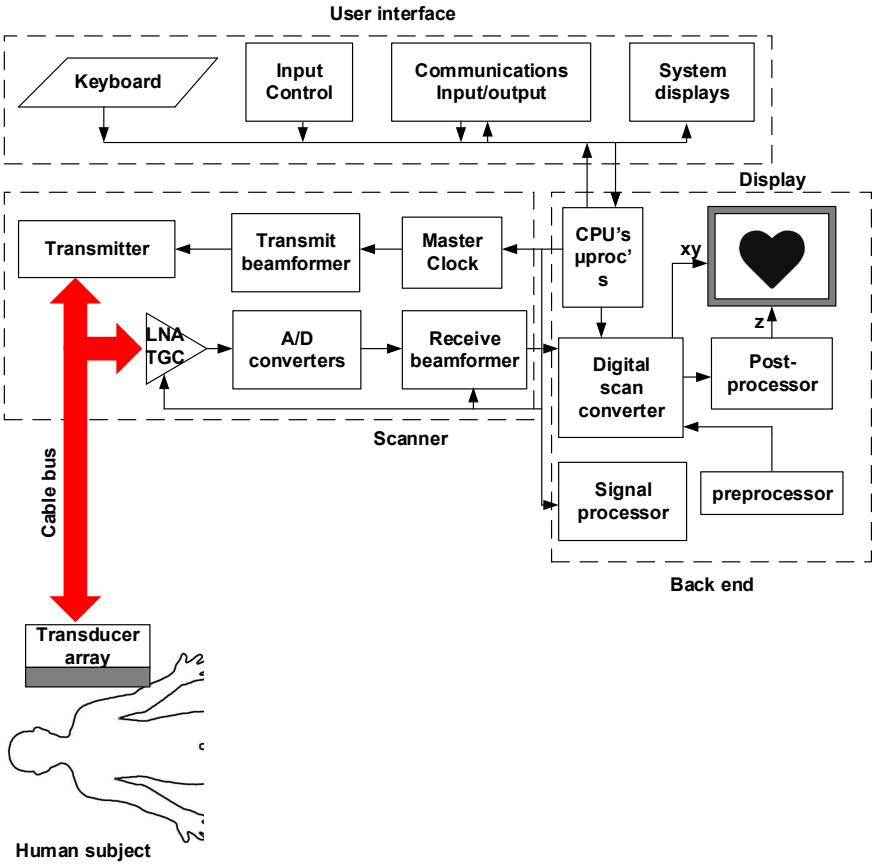

Figure 1.2: Block diagram of a typical medical ultrasound imaging system [8].

electric materials are simply diced and bonded to a backing layer. A typical ultrasound system consists of an interface, display, back-end and scanner unit. Block diagram of a typical ultrasound system is shown in Figure 1.2. Operator can provide instruction to the machine using the user interface. All the receiver electronics, Time Gain Compensation (TGC) circuits, Analog to Digital Converters (ADCs), receiver beamformer, high voltage transmitter and transmit beamformers are placed in the scanner block. Electrical connections to the array are done through long cables from the scanner. Data from the scanner unit are processed by the back-end unit for display.

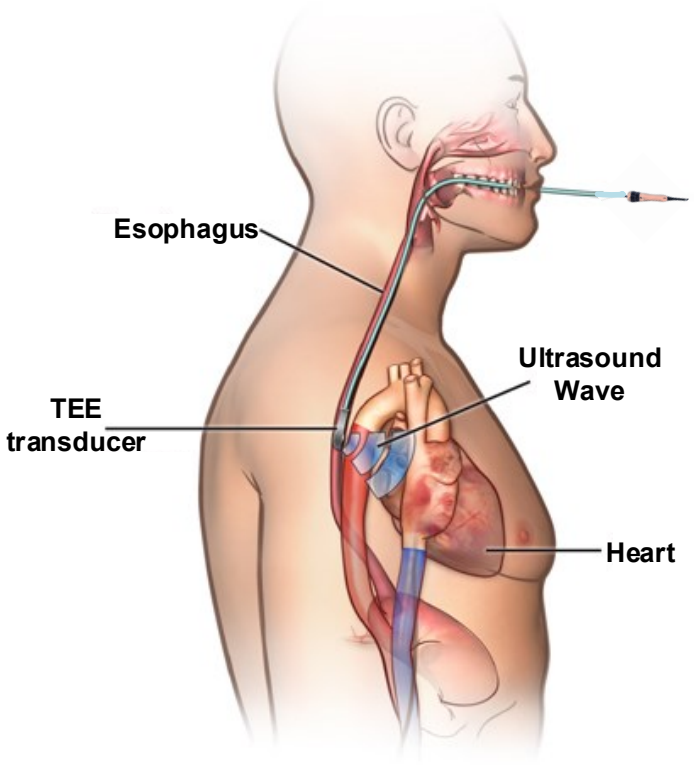

Figure 1.3: Transesophageal Echocardiography procedure.

1.2 Ultrasound for Medical Heart Imaging

Heart disease is the number one cause of deaths worldwide; 1 in 9 deaths in the United States are due to heart failure. Mortality rates due to heart failure are declining as evidence-based approaches for treating heart diseases are emerging [14]. Many interventional procedures of the heart, such as aortic valve replacement, atrial septal defect closure and intracardiac occluder placement can now be performed by minimally invasive surgery with the help of catheterized ultrasound imaging guidance [15]. Two commonly used procedures to image human heart are transesophageal echocardiography (TEE) and intracardiac echocardiography (ICE). TEE and ICE procedures are used for real-time detailed images to guide cardiac interventions [16]. They have become an important clinical tool for guiding electrophysiology to treat arrhythmias and for structural heart procedures to treat defects in heart valves, holes in heart

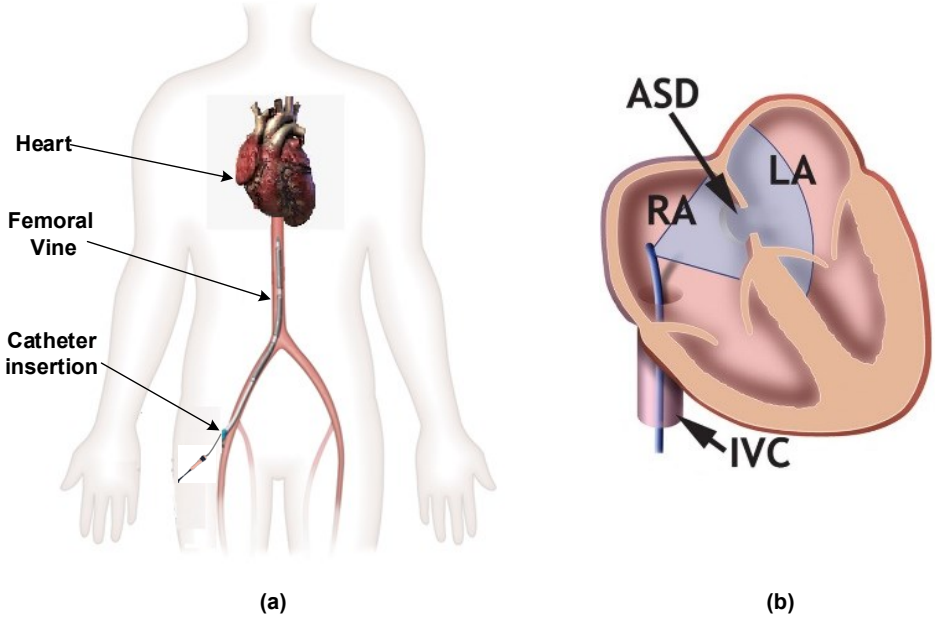

Figure 1.4: (a) ICE catheter insertion inside human body (b) ICE probe inside the heart.

wall, heart muscle diseases and valve replacement [17, 16, 18, 19].

TEE is performed by passing the ultrasound probe down the esophagus (food pipe) near the heart. Pulse echo images of the heart are generated using the ultrasound probe. The patient usually needs to be under general anesthesia during the whole procedure. Figure 1.3 shows how TEE probe is placed near the heart for imaging.

Similar to TEE, the ICE catheter has a small ultrasound imaging probe at the tip. In order place the ICE probe inside the human heart, physician makes a small incision near the upper part of the leg and inserts the ICE catheter inside the femoral vein. The catheter tip is then navigated through the femoral vein to the Inferior Vena Cava (IVC) and positioned into the right atrium of the heart. Using pulse echo ultrasound imaging technique, 2-D cross sectional image of the entire heart is obtained using the ICE probe. Figure 1.4 shows how ICE probes are inserted and navigated inside human body.

During the procedure, both the TEE and ICE catheters are guided using X-ray

fluoroscopy. ICE catheters provide a unique method to image the inner workings of the heart [20] and has been replacing TEE in some applications [21, 22, 23]. The main advantages of ICE over TEE are it can be performed without the need of general anesthesia and procedure time can be shorter. ICE uses 8F to 10F catheters which can be navigated through the femoral vein. The ultrasound frequency range of the ICE is 5 MHz to 8 MHz and has a penetration depth of 10 cm with lateral resolution of 1 to 2 mm, better than TEE.

Catheter based real-time 3-D imaging systems such as 3-D transesophageal echography (TEE), require data to be captured from a 2-D array with many transducer elements simultaneously to avoid motion artefacts [24]. In ICE imaging catheter applications, gathering the data from large number of element transducer arrays is extremely challenging with standard interconnect and transducer technology as there is a restriction on cable count due to the diameter of the catheter [25]. Current commercial ICE catheter (ACUSON AcuNav^{TM}) [26] utilizes a 64 element 1-D phased array and can provide only 2-D images. Newer ICE catheter AcuNav^{TM} V provides limited-volume 3-D real-time volumetric images of the heart structure [27, 28]. Each element of the 1-D array is connected to the back-end image processing system with individual cable. It is extremely challenging to put more cables trough the catheter. As a result, if conventional method is followed, element count cannot be increased too much further. But to obtain 3-D images with sufficient image resolution the ultrasound array needs to have a high-density 2-D array with a large number of elements. As shown in Figure 1.5, a 1-D array can only generate 2-D image and 2-D array can produce 3-D images. The element count of a 2-D array can very high. Current 2-D TEE arrays have 2500 elements. To eliminate the need for a large volume of interconnects between the transducer array and the signal processing unit, electronics can be placed adjacent to the transducer array. Figure 1.6 shows the modified block diagram of an ultrasound system which requires less number of cables as transmit beamformer

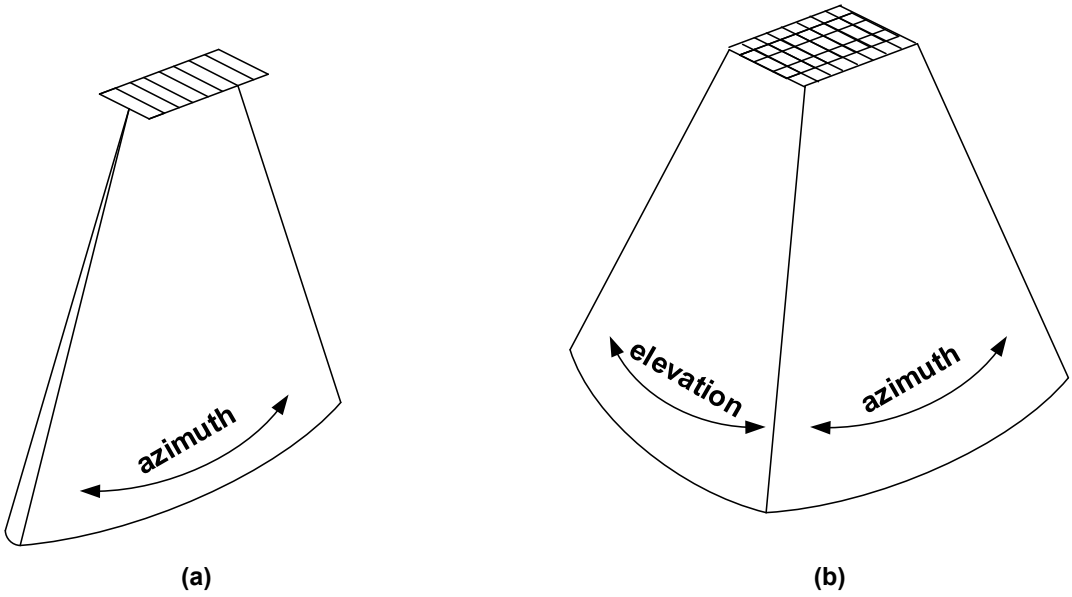

Figure 1.5: (a) 2-D scan from an 1-D phased array (b) 3-D scan from a 2-D array.

and receiver multiplexer are placed of the transducer side. Also mentioned earlier ICE requires X-ray guidance [29] which causes exposure to harmful radiation to both patients and physicians. The disadvantages of X-ray imaging can be avoided if the ICE catheter can be designed to operate under MRI with proper markers. In order to bring 3-D ICE technology into MRI guided intervention domain, the number of cables in the catheter should be reduced dramatically to control catheter heating [30] while keeping the real-time imaging capability. Current approaches to cable reduction tend to rely on area and power-hungry circuits to function, making them unsuitable for use in catheters. By using the CMUT-on-CMOS technology [31] or other multi-chip packaging technology [32] [33] [34] [35], one can incorporate on-chip electronics. With these approaches, CMOS transmitter beamforming and driver electronics can be integrated on chip to eliminate a significant number of electrical cables for transmit beamforming. If one can also implement massive on-chip multiplexing of the receive channels this can provide a unique platform for real-time 3-D ICE catheters under MRI as well as X-ray. This approach can also be used in 1-D ICE catheters to reduce

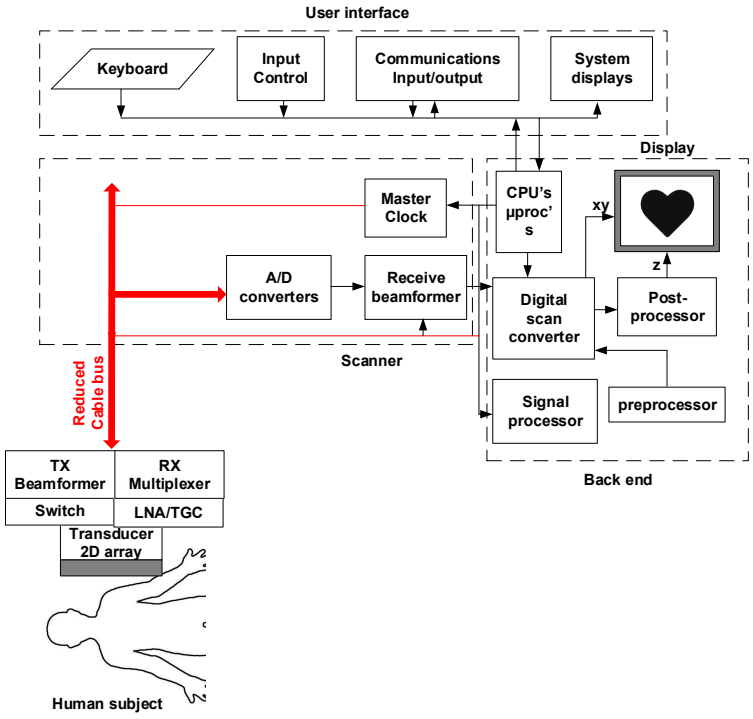

Figure 1.6: Block diagram of a modified ultrasound system to reduce cable count form the transducer array to scanner.

the number of cables.

For high-density imaging arrays required for ICE or TEE, the piezoelectric transducer arrays are placed over an Application Specific Integrated Circuit (ASIC) to avoid large number of cables, which can be called piezo-on-ASIC approach. The most recent example of this approach is a 3-D imaging ICE catheter developed by GE, in which over 800 elements of a 2-D array are placed over a 3 mm x 7 mm ASIC and 88 cables are used to connect the catheter to the imaging system [36]. The approaches that are developed in this thesis would be applicable to both CMUT-on-CMOS or piezo-on-ASIC approaches.

An important aspect of this thesis depends on the real-time data processing of the ultrasound data. In the last quarter of the 20^{th} century Field Programmable Gate Array (FPGA) based digital signal processing (DSP) has opened the possibility to do real-time image processing with large amounts of data from high-density ultrasound

transducer arrays with large number of elements. While modern digital electronics allow real-time image processing, the quality of the image mainly depends on the signal quality and fidelity of the transducer and analog front-end electronics (AFE). Therefore, special attention needs to be paid while designing the AFE so that it meets the bandwidth, SNR and dynamic range requirement of the system.

1.3 Receiver Array Cable Reduction Techniques

1.3.1 On-chip ADCs

There are multiple approaches to reducing cable count that were considered for high-density ultrasound imaging arrays. One option is on-chip digital modulation. Such a system would require integration of Analog to Digital Converters (ADC) with the AFEs of the ultrasound transducers. The integration of ADCs will allow smart signal processing for reducing the number of interconnects between the transducer array and the signal processing unit. On chip ADCs are possible, for example [37] presents an 8 channel 10-bit pipeline ADC which occupies approximately 4 mm^2 requiring almost 330 mW. However, in a size and power constrained system, such as an ultrasound imaging catheter, this would be simply unfeasible to implement.

1.3.2 μ-Beamformer

Another approach, which has been demonstrated in [36, 38, 39, 40, 41, 42, 43], involves performing partial beamforming (μ-beamforming) with analog delay chains in the transducer. μ-beamforming is performed by delaying the signals relative to each other in such a way that signals from a certain focal point, arrive simultaneously and can be coherently summed. By performing delay-sum beamforming in the transducer side, fewer cables are required as the raw signals from every element do not need to be transferred for processing. Beamforming can be performed in either analog or digital domains. For high-density large number element applications, analog beamforming is

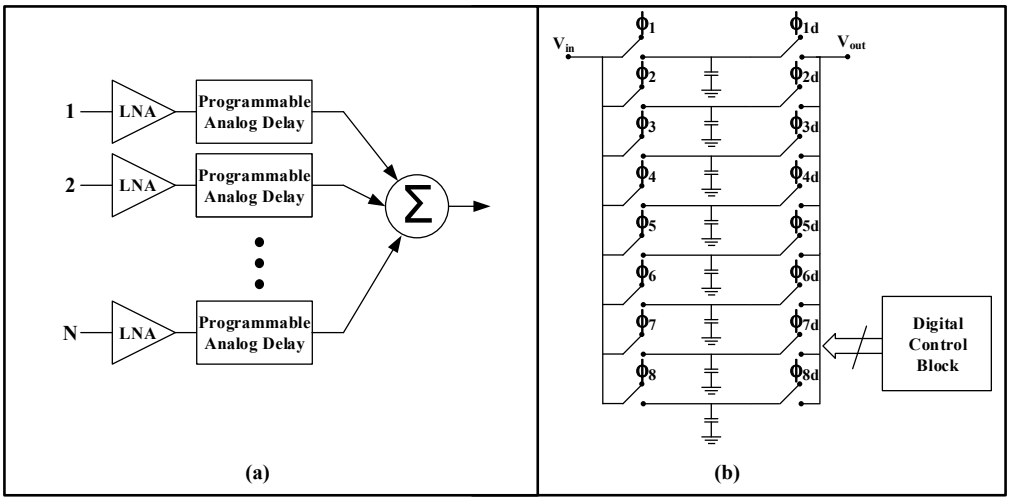

Figure 1.7: (a) Block Diagram of a μ-Beamformer architecture (b) Schematic of an analog delay circuit.

preferred due to cost, power and size constraints. But analog beamforming requires a large number of capacitors and switches for each channel in order to achieve the required high-resolution analog delays. This cable reduction technique is applicable for hand-held ultrasound devices and TEE probes but for heavily area limited systems like catheter based ICE probes it may be unsuitable. This method would also be incompatible with systems which make use of advanced imaging techniques requiring collection of all raw echo data.

1.3.3 Pulse width Modulation (PWM)

An effort was made to reduce the cable count for ultrasound catheter probes by using a PWM technique as reported in [44]. PWM employs a train of pulses where the signal is sampled and each sample value is encoded in the width of a pulse. Once converted to duty cycle, the information becomes more immune to channel noise and attenuation. Furthermore, PWM requires less area and power than ADCs [45]. One major disadvantage of PWM technique is that it requires very high channel bandwidth to transfer data from the PWM source to the signal processor. For example, to send

8 channels with 10 MHz band limited signal with 60dB dynamic range via one cable, the required bandwidth of the receive channel needs to be at least 160 GHz. Cables with such high bandwidth are not feasible to be placed inside the catheter due to its diameter restriction. Also, real-time processing of such large volumes of data will be extremely challenging.

1.3.4 Static Channel Multiplexing

In this method, a signal receive element in the array is connected to the cable for a full firing. On each subsequent firing the next element is connected, and so on until data for each element has been collected. This approach has been demonstrated in several systems [46, 47, 13]. While this allows for cable reduction, it also means that during image reconstruction motion artifacts shall appear while imaging a dynamic object as one element can only be sampled in each firing. Also for system with many elements this method can reduce the frame rate as more firings would be required to get the data to generate a single frame.

1.4 Transmitter Array Cable Reduction Techniques

While techniques for reducing the number of cables for ultrasound receiver arrays were reported, some architectures of on chip transmitter beamformer have also been published recently.

1.4.1 Column-Row-Parallel Beamformer

A Column-Row-Parallel on-chip transmit beamformer was reported in [48]. Using this architecture with 2-D arrays, plane wave ultrasound beams can be steered. However, it has much less flexibility for producing focused beams as the delays can only be programmed row by row or column by column. The beamformer can be programmed at high speed, but requires the number of cables to increase proportionally with the

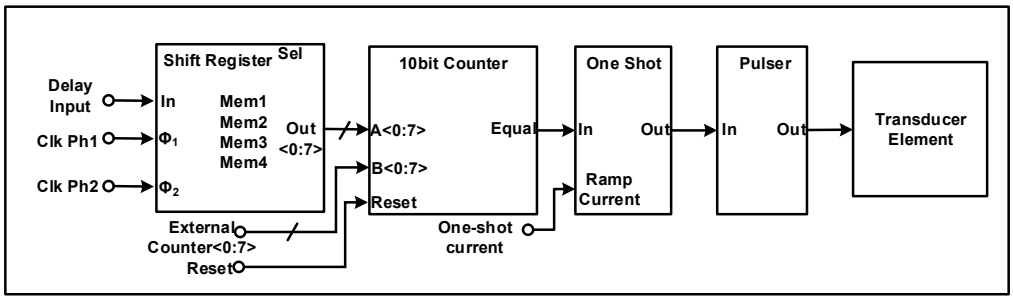

Figure 1.8: Transmit beamformer block diagram published in [32].

number of elements in the width or length of the array.

1.4.2 Programmable Shift Register and Comparator Beamformer

An on-chip beamformer was described in [32] is shown in Figure 1.8. The beamformer uses shift registers to store the delay value for each transmitter. Before beams are transmitted the shift registers are programmed with delay values. After all the shift registers are programmed, an external counter starts counting. A comparator compares the value of the stored delay value and external counter value and sends signal to the one-shot circuit when the values matches. The one-shot circuit, drives the on-chip high voltage pulser to fire pulse. The one-shot circuit consists of a current-starved invertor chain to set the pulse width. An external cable is used to set the current of the one-shot circuit. By storing the appropriate delay values to each register, the ultrasound beam can be steered and by setting the one-shot circuits control current the pulse width can be set. This architecture requires a number of RF cables to send the counter data to the on-chip beamformer. Also, the pulse width control analog signal can be effected by the clock and control signals, resulting in a change in the desired pulse width.

1.4.3 Beamformer with an Integrated Counter

A beamformer with integrated counters was introduced in [33]. The beamformer controls the delay of pulses by programming shift registers and comparing the stored value with the integrated common counters value. Integration of counter reduces cable count with the cost of some silicon area. For pulse width control this architecture uses a 6-bit programmable counter and comparator for each transmit element which occupies significant area. Instead of using counters for each transmit element, it is possible to use a global programmable counter to control the pulse width. Thus, the silicon area can be reduced to place the beamformer on the tip of the catheter.

Previously reported literature focused mostly on either cable reduction on the receiver side [38, 39, 40, 41, 42, 43, 44] or on the transmitter side [32, 33, 48]. But it is not particularly advantageous unless both the transmit beamformer and receiver cable reduction electronics with small area are integrated at the catheter tip while connected to the outside system with a reduced number of cables. In the 3-D imaging ICE catheter described in [36], transmit beamformer and receiver μ-beamformer circuits are successfully implemented, but details of the ASIC design and implementation and cable requirements are not provided. This research explores the design of the CMOS receiver circuitry which implements a Time Division Multiplexing (TDM) scheme to address the receive cable restrictions of the catheter and, using a digital demultiplexing technique, allow for a reduction in the number of analog signal processing stages required. Also, we explore an on-chip programmable transmit beamformer circuit which can reduce the cable requirement for producing focused beams.

The thesis is organized as follows: In Chapter 2, we first describe a fully programmable 16 pulser transmit beamformer architecture and provide details of its operation with a high voltage pulser along with its characterization with a 1-D CMUT array. In Chapter 3, we describe the analog front-end (AFE) electronics and present

experimental characterization results of its components. In Chapter 4, we first discuss an 8×1 Orthogonal Frequency Division Multiplexing (OFDM) scheme for receive cable reduction and describes it limitations. Then in the same chapter we introduce implementation of an 8×1 TDM with direct digital demultiplexing for receiver cable reduction. In Chapter 5, we describe an imaging experiment setup where we combine a 32×4 TDM receiver and programmable 16 pulser transmit beamformer IC with an 1-D CMUT array on a single PCB and collect imaging data from a wire target. Chapter 6, we introduce another novel transmit beamformer architecture. This beamformer is capable of transmitting Doppler pulses and width of individual pulses can be programmed for apodization purposes. The data for programming the beamformer and the clock can be sent via single cable by encoding the data in the pulse width of the clock. The data can be decoded using sense amplifiers thus eliminating the requirement of any on-chip PLL. A current efficient high voltage pulser is also introduced in the new beamformer. Detailed operation the beamformer and electrical test results are presented in the chapter. We also describe transmit receive monolithically integrated chips for both a 1-D and a 2-D sparse array. Finally, in Chapter 7, we conclude the thesis with discussions for future implementations.

CHAPTER 2
TRANSMIT BEAMFORMER

An area efficient on-chip transmitter beamformer with low cable count needs to be designed so that overall system can be implemented in a catheter based ultrasound system. In this research, a reconfigurable on-chip high voltage transmitter beamformer is designed. Using the beamformer the transmitted beams can be steered and focused as show in Figure 2.1.

2.1 Transmit Beamformer Architecture I

The beamformer I consists of a global programmable down counter and another global down counter and a global shift register for controlling the data loading. The implemented beamformer consists 16 high voltage pulsers, one for each element. Each pulser consists of an 8-bit shift register to store the delay value, two comparators, a digital pulse shape generator and a 30V pulser. A 4-bit lock register and comparator which detects a specific bit pattern is implemented to ensure once proper data is loaded then no more data can enter during a firing. The block diagram of the implemented beamformer is shown in Figure 2.2. The implemented circuit was programmed and operated at 200 MHz speed with the help of an FPGA via μ-coax cables.

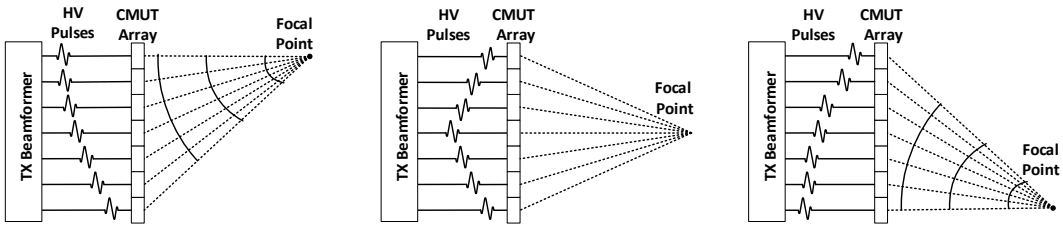

Figure 2.1: Transmit beam steering.

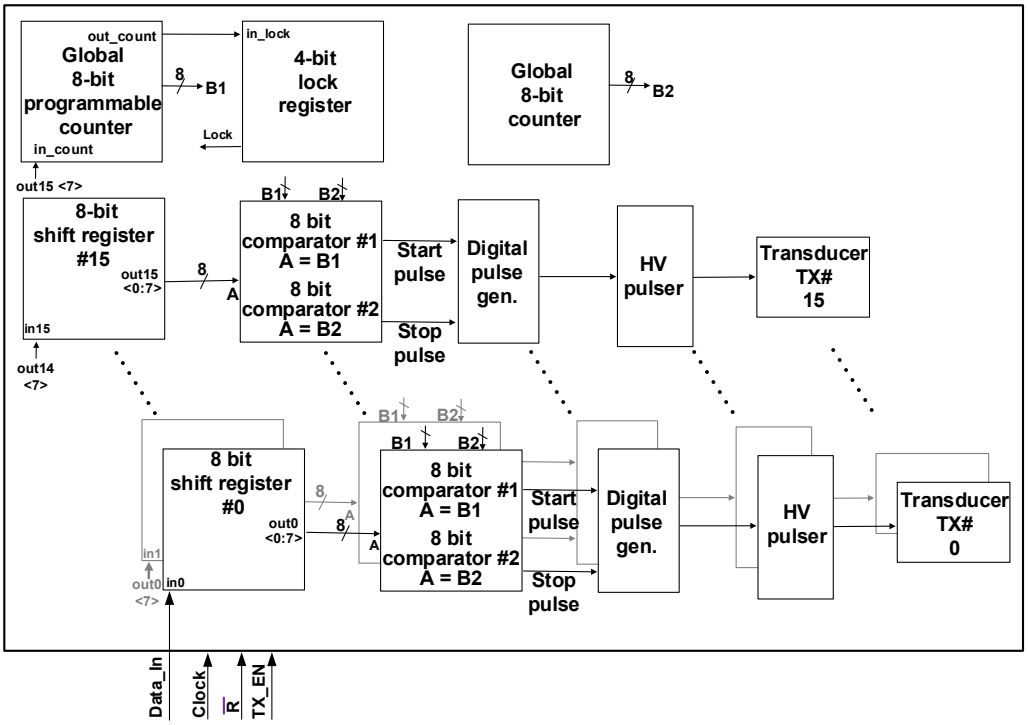

Figure 2.2: Block diagram of the implemented transmit beamformer architecture I.

2.1.1 Programming the Beamformer

Two external signals **TX_En** and $\overline{\mathbf{R}}$ are used to control the programming and firing cycle of the beamformer. Before programming the beamformer, all the register and counters are cleared by asserting the external **TX_En** and $\overline{\mathbf{R}}$ signals low. After resetting the registers and the counters, the **TX_En** signal is set high and the programming data is sent from the FPGA via a μ-coax cable through the Data_In pin of the Transmit beamformer. Figure 2.3 shows the configuration of the register during the delay values are programmed. After the reset, the output of the AND4 of the 4-bit lock shift register is low and data can be shifted through the registers for programming the delays as shown in Figure 2.3. The first 4 bits of the data are used as preamble bits (1111_2) and when they reach the 4-bit lock registers the output of the AND4 becomes high and data loading stops and the counter and registers are

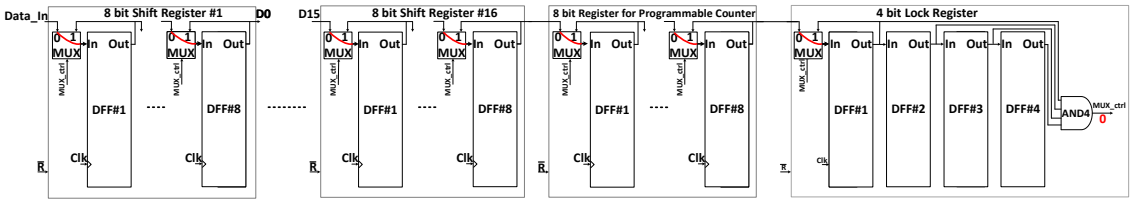

Figure 2.3: Register configuration while beamformer is programmed.

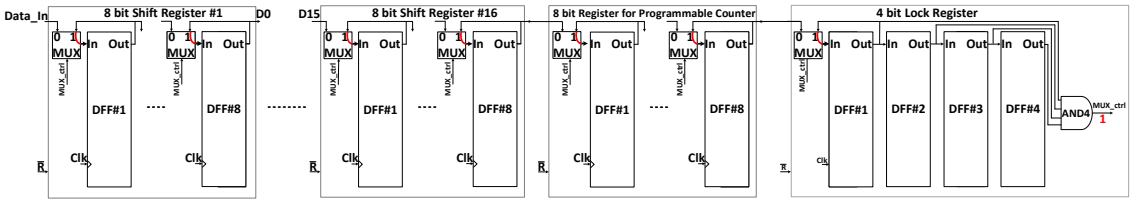

Figure 2.4: Register configuration after beamformer is programmed.

programmed with appropriate value. Figure 2.4 shows the configurations after data are loaded.

During each programming cycle, a 140-bit ($16 \times 8 + 8 + 4 = 140$) long data packet needs to be sent to program the entire beamformer. The first 4 bits of the data packet are used as preamble bits (1111_2) which, when they reach the 4-bit lock registers, the output of the AND4 becomes high and data is stopped. This then triggers the counter and registers to be programmed with appropriate value. After data has been loaded the $\overline{\mathbf{R}}$ signal is set to high and the counter starts counting.

There are two on-chip common down counters used in the beamformer for pulse timing. To control the pulse width, the start value of one of the counters can be programmed and the other down counter always starts counting from highest value 11111111_2. After data has been loaded the internal counter starts counting. The timing diagram for the beamformer operation is shown in Figure 2.5.

2.1.2 Pulse Width Controller

The values of the stored registers are compared with the counter values once they start counting. When the value stored in a register matches the value of the programmable

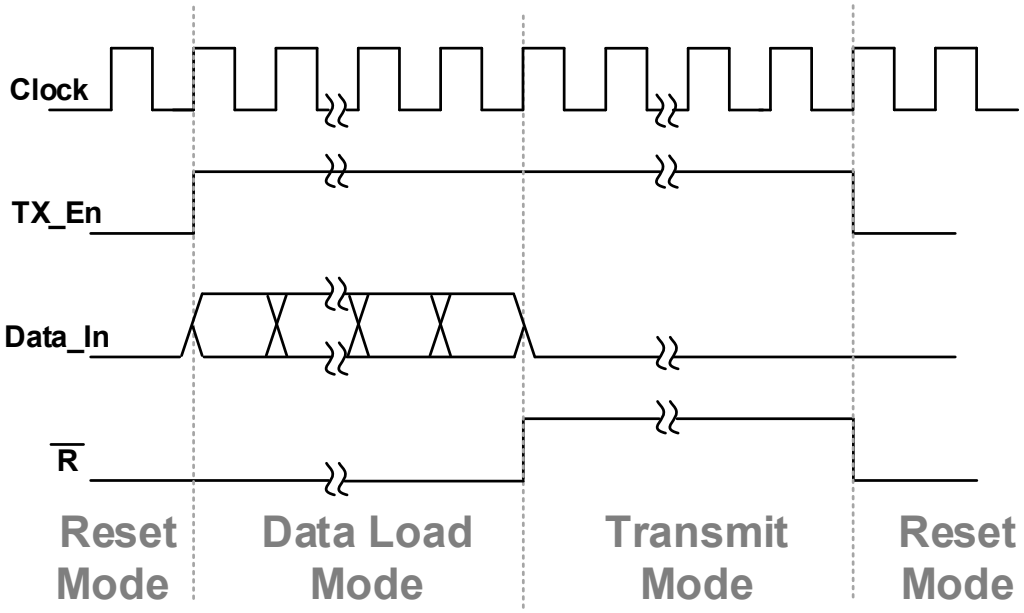

Figure 2.5: Timing diagram of beamformer programming and transmit.

counter then the comparator sends a start pulse to the pulse generator to trigger the start of the high-voltage output pulse. When the register value matches the other counter, a second comparator sends a stop pulse to the pulse generator which ends the high-voltage output. Thus, the difference between the start value of the programmable counter and the non-programmable counter determines the pulse width and difference between the stored value of shift registers and programmable counter determines the delay of the pulse. The circuit for the digital pulse generator is shown in Figure 2.6.

As an example, if a pulse width of 45 ns and delay of 200 ns are required for a particular pulser, then the start value of the programmable counter is set to 11110110_2 and value of the corresponding register for the pulser is programmed to 11001110_2. After programming the registers, the $\overline{\mathbf{R}}$ signal is deasserted and the counter starts counting down at 200 MHz frequency. The programmable counter takes 40 cycles or 200 ns to reach 11001110_2. Once the programmable counter reaches this value,

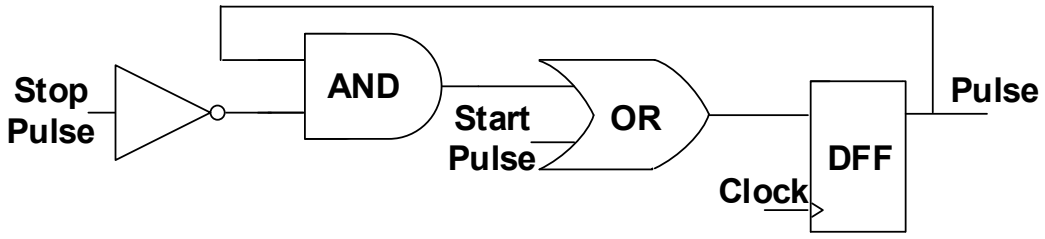

Figure 2.6: Implemented pulse generator circuit.

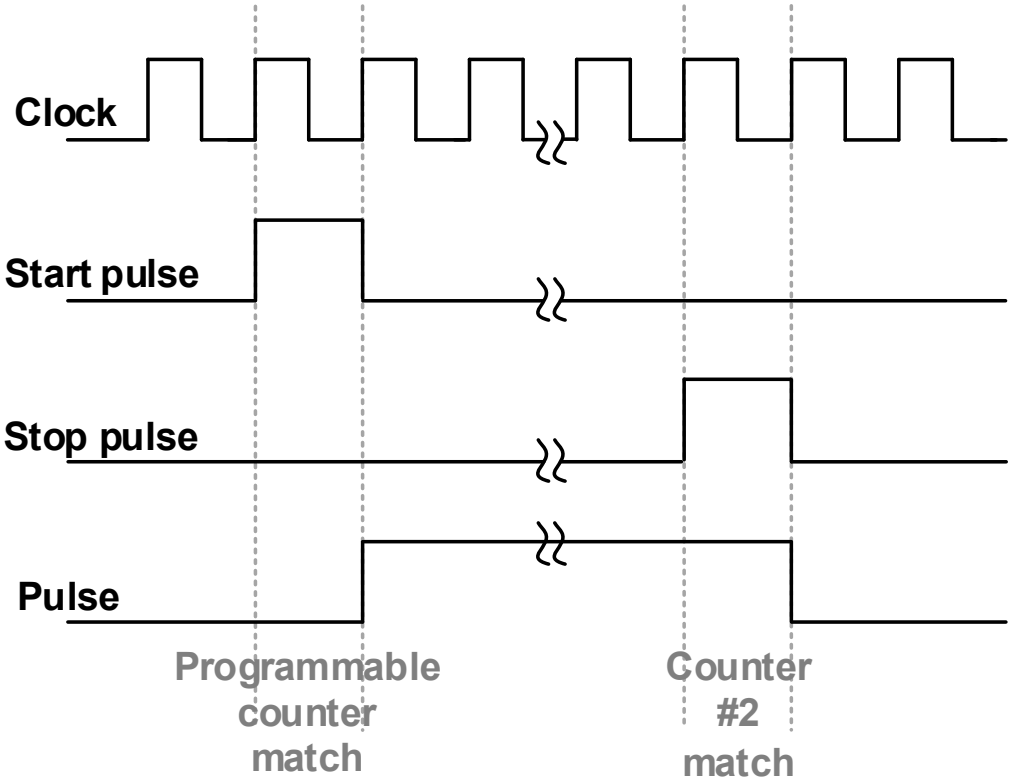

Figure 2.7: Timing diagram of pulse generator.

the start comparator corresponding to the pulser sends a start pulse to the pulse generator and pulse starts. The non-programmable down counter takes 49 cycles or

245 ns to reach the value 11001110_2. Once it reaches the value, the stop comparator corresponding to the particular pulser sends a stop pulse to the pulse generator and pulse stops. The timing diagram for the circuit is shown in Figure 2.7. In the diagram, the timing of the start pulse can be adjusted by changing the value of the programmable counter thus the pulse width can be adjusted. In this beamformer, the delay and pulse width can be adjusted with 5 ns resolution, limited by the clock period. Each element must share a common pulse width in this design as they each share the same counters to reduce overall area.

In [32] an analog pulse width controller is used which requires a large capacitor and occupies significant area. The previously reported digital pulse shaper controller in [33] requires a 6-bit counter in each pulser element to control the pulse width which occupies significant area. By using the two-global counter approach discussed in this beamformer, the area can be significantly reduced, making this design more suitable for ICE application where silicon area is highly limited.

2.1.3 High Voltage Pulser

The low voltage output of the digital pulse generator is fed to the input of a High Voltage (HV) pulser. The circuit diagram of the HV pulser is shown in Figure 2.8. The HV pulser uses a 1.8 V to 5 V level shifter to drive the 30 V output transistor at a faster speed. The output transistors are designed to drive 22 pF capacitive load with a rise and fall time <20 ns due to the element size. For lower capacitance elements, smaller transistors can be used allowing faster slew rates to be achieved.

2.1.4 System scalability

The designed beamformer can be easily scaled up by adding additional cells for each element - cells consisting of a single delay register added in to the shift register chain, a pulse width controller and HV pulser. The maximum delay for the 16-element array,

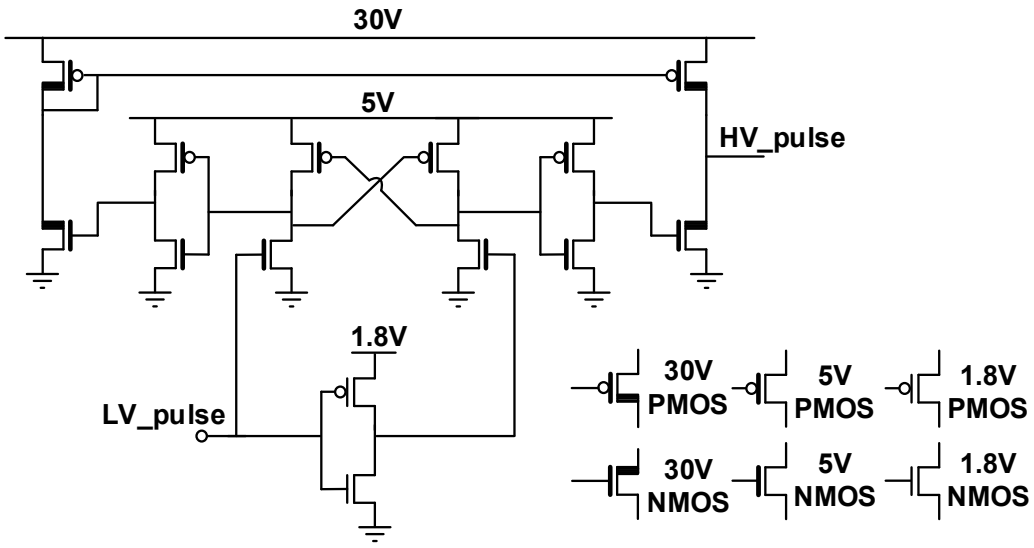

Figure 2.8: Circuit diagram of the implemented HV pulser.

in the case when the array is steered to 45° angle, is calculated approximately as 800 ns based on the speed of sound in water and the element sizes, which can be achieved by using an 8-bit counter. The beamformer can be modified to handle a larger arrays, such as a 64 elements, by changing the 8-bit counters and delay registers to 10-bits considering the required maximum delay. In this design, the layout height of the HV pulser is more than the low voltage delay registers. Therefore, the additional 2-bits for registers and counters can be placed in the empty space of the low voltage circuits without increasing the circuit pitch size.

2.1.5 Beamformer I Characterization Experiment

A prototype of the 16 channel beamformer I IC was designed in TowerJazz 1P4M HV process and occupies a 3.22 mm × 0.9 mm area (without the bond pads). Figure 2.10 shows the micrograph of the fabricated beamformer-I.

The fabricated beamformer I IC was diced and wire bonded to a PCB to properly power and connect the clock and control signals to the circuit.

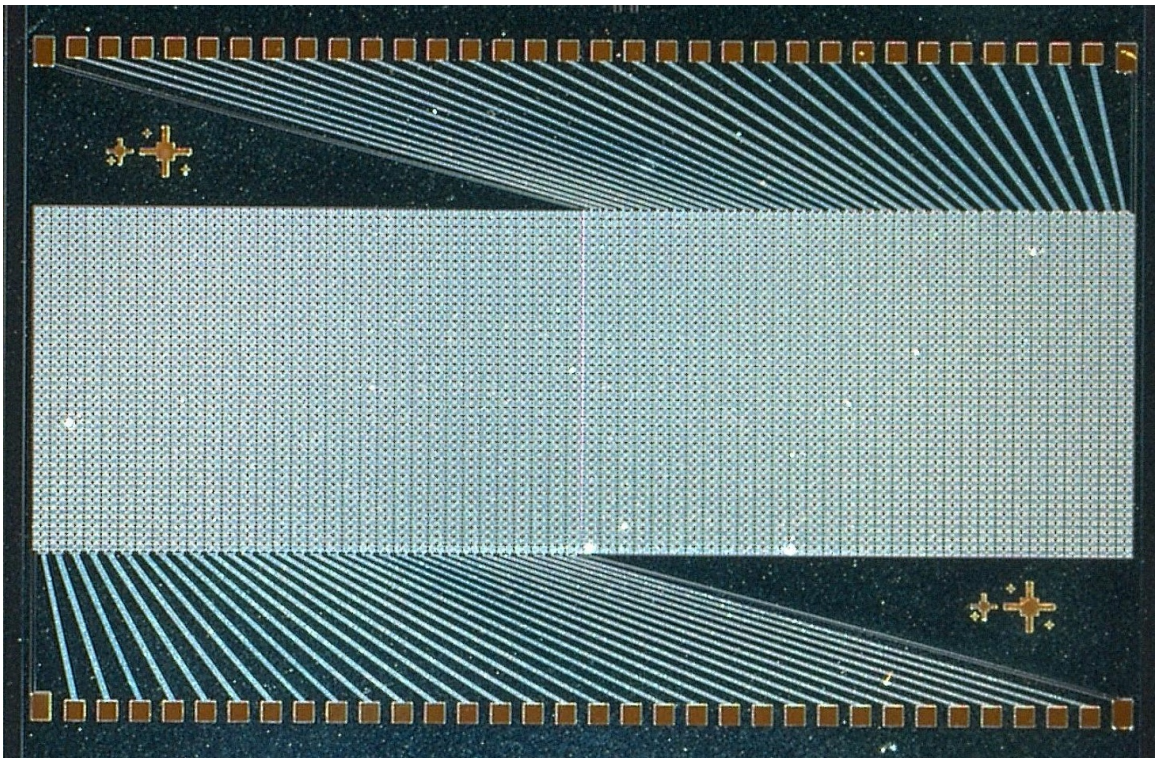

Figure 2.9: Micrograph of the CMUT array.

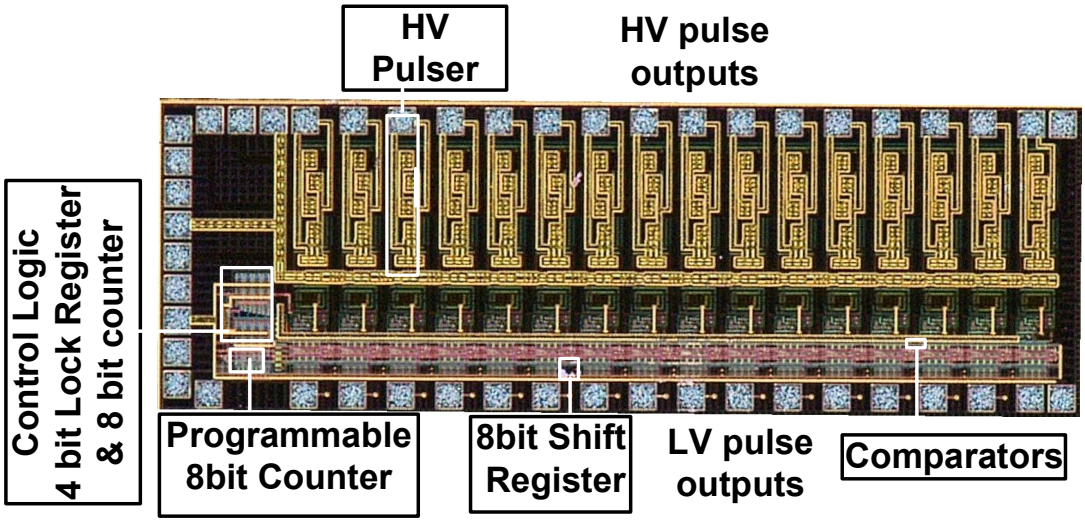

Figure 2.10: Micrograph of the beamformer I IC. Area 3.22 mm $\times$ 0.9 mm.

The CMUT arrays used to validate the functionality of the beamformer design are fabricated as a 64 element 1-D array. The array elements comprise 80 membranes having a length of 2 mm in elevation direction with 104 μm element pitch (Figure 2.9).

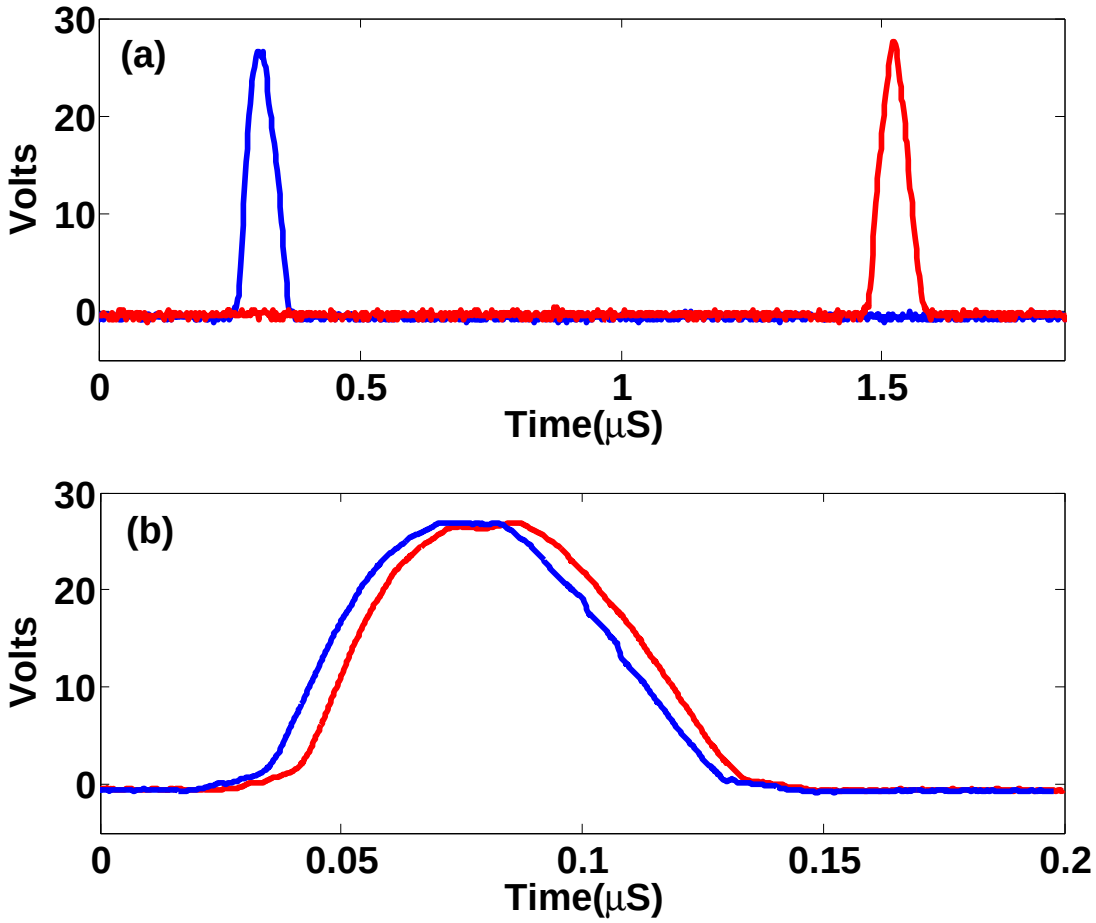

Figure 2.11: (a) High voltage pulse with relative maximum delay of 1.27 μs and (b) with relative minimum delay of 5 ns.

Each square shaped membrane is 46 μm $\times$ 46 μm in size resulting in 8.5 MHz center frequency with 80% fractional bandwidth. Silicon Nitride (Si_3N_4) is used for the dielectric isolation layer with a thickness of 200 nm and the total Si_3N_4 membrane thickness is 2.2 μm. AlSi is sputtered as top electrode which has 80% of membrane coverage. The membranes have a vacuum gap of 95 nm which results in about 25 V collapse voltage for the device.

For the initial testing the data, clock and other control signals were sent via 1 meter length of 75 Ω, 48 AWG μ-coax cable with 0.17 mm outer diameter, as could be used in a catheter application, to ensure the results take into account the realistic effects of a bandwidth limited channel. During the test, focused and defocused beam profiles with

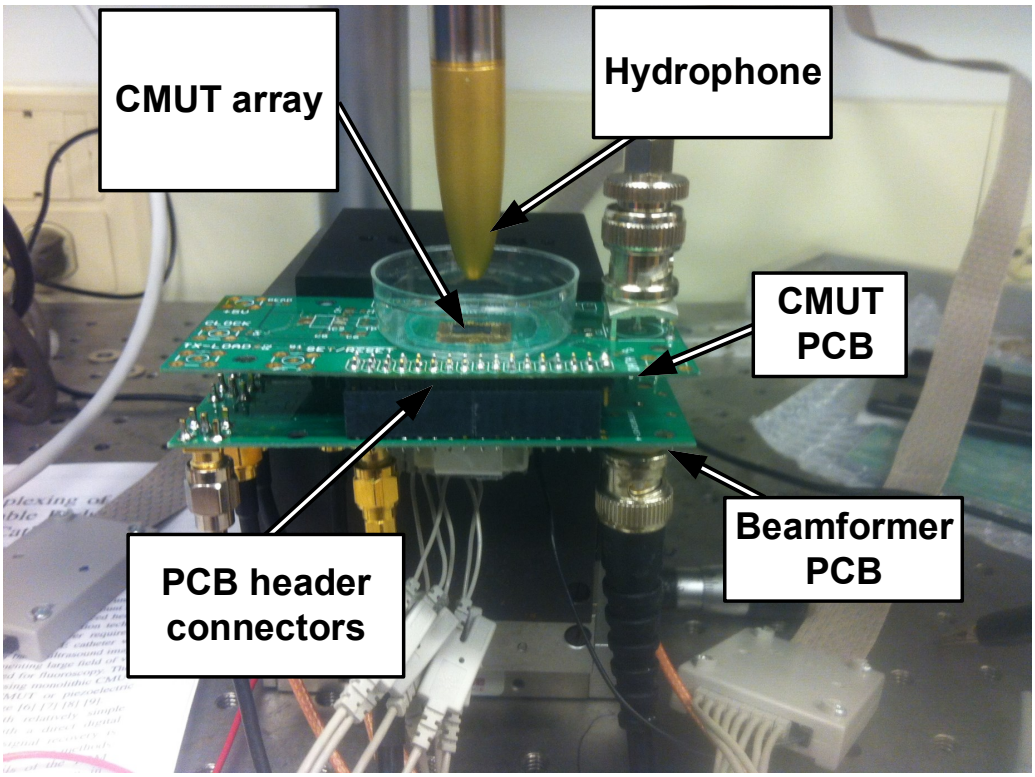

Figure 2.12: Test setup for the beamformer characterization.

a pulse width of 55 ns were generated. The data, clock and the control signals for beam generation were produced by a Stratix V GS FPGA (Stratix 5SGSMD5K2F40C2N, Altera Corp., San Jose, CA). The low voltage outputs of the pulse generator which are fed out to test pads were captured with the 16 digital inputs of an Agilent MSO7104A oscilloscope (Agilent Technologies Inc., Santa Clara, CA). The low voltage outputs of the pulse generator were captured with 16 digital inputs of Agilent MSO7104A Oscilloscope simultaneously. Figure 2.13(a) and (b) show the captured 16 low voltage outputs from the beamformer for a defocused beam focused beam, respectively. The delay resolution was measured. The relative delay from one element to another can be programmed from 0 to 1.27 μs with 5 ns increment (based on a 200 MHz clock). Figure 2.11(a) shows programmable relative maximum delay of 1.27 μs between two

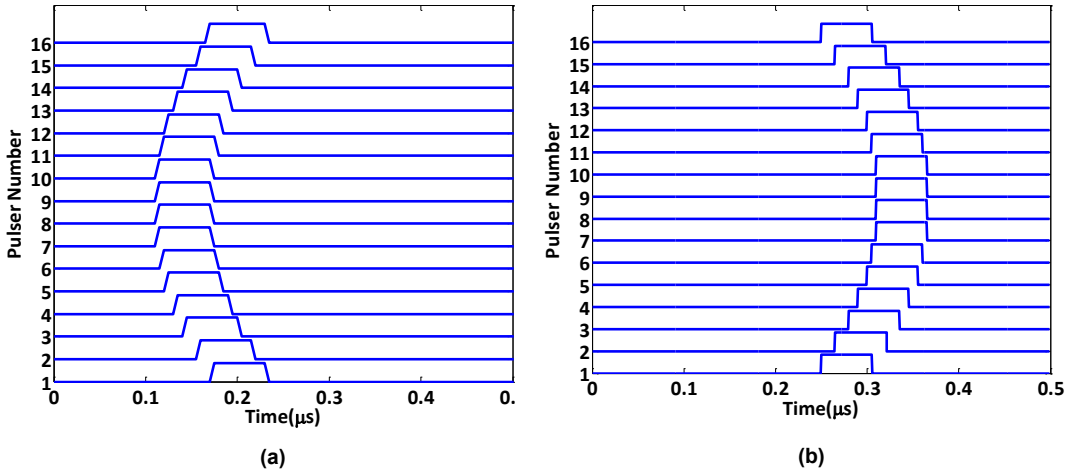

Figure 2.13: Low voltage pulses generated for (a) defocused (b) focused beam.

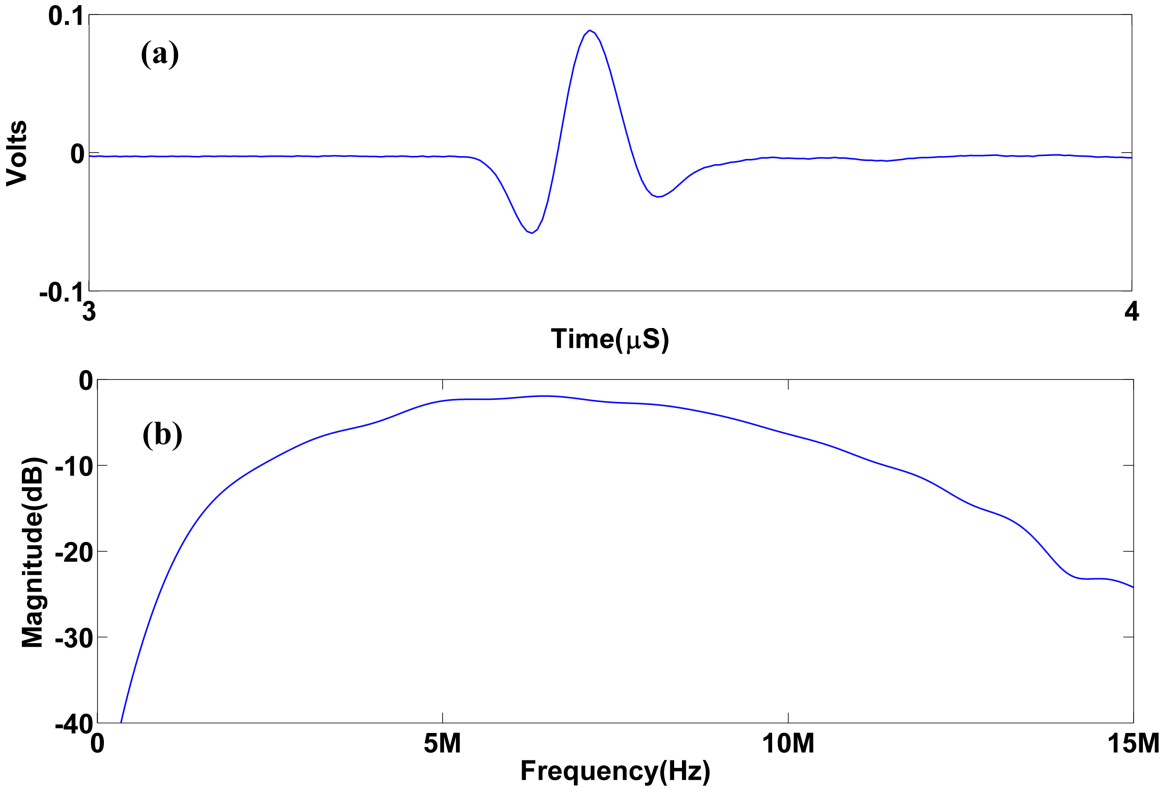

Figure 2.14: (a) Captured hydrophone signals of a 70 ns pulses. (b) Corresponding frequency responses of the captured signals.

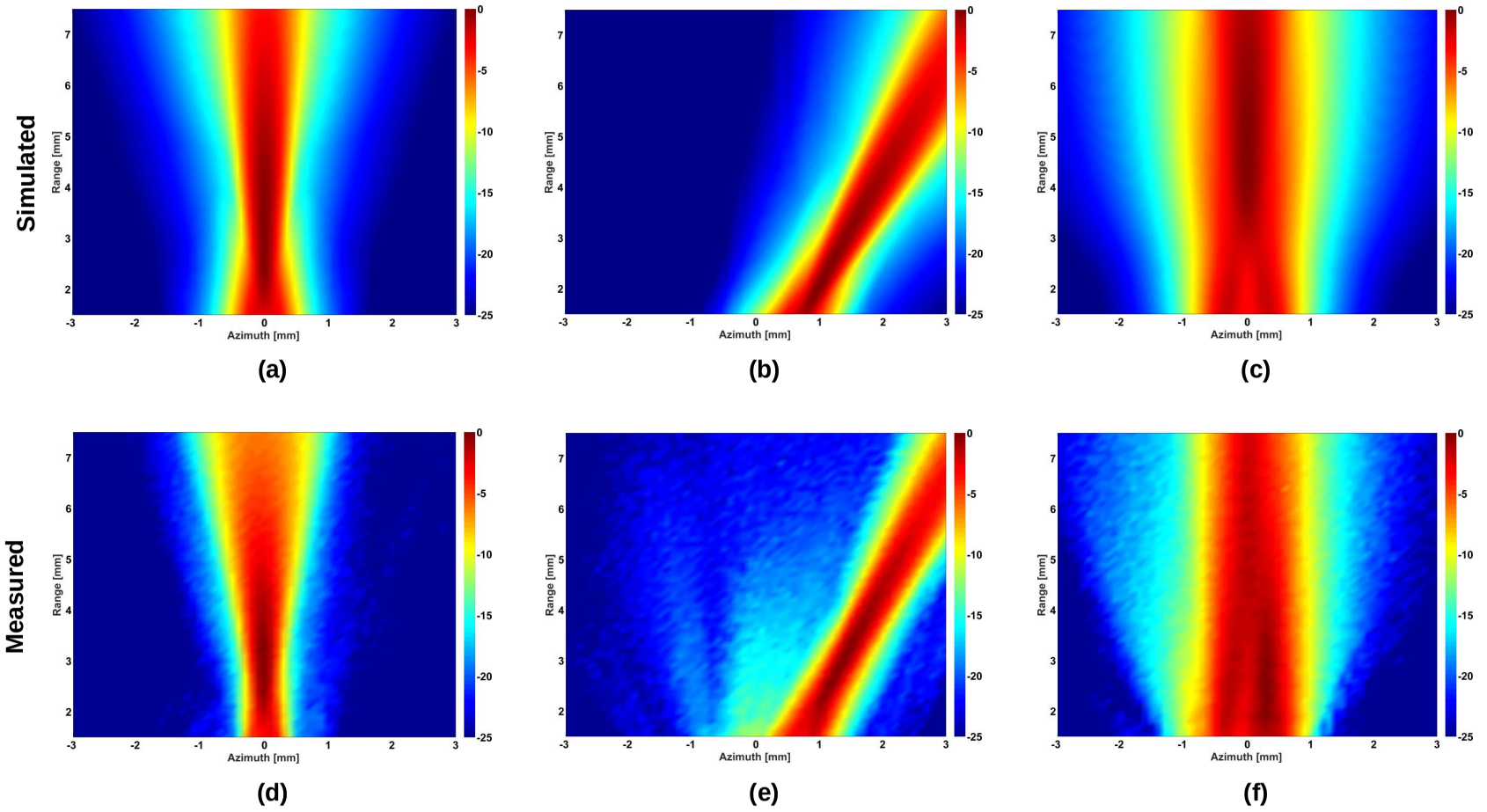

Figure 2.15: Simulated (top) and measured (bottom) beam patterns for non steered focused beam (left), steered focused beam (middle), and plane beam (right).

pulses and Figure 2.11(b) shows two high voltage pulses with delay of 5 ns. The amplitude difference between the two pulses in Figure 2.11(a) is due to resistive losses inside the beamformer IC which can be reduced by increasing the power trace width in the final design.

Immersion experiments were performed to characterize and test the performance of the fabricated beamformer with the CMUT array. 16 elements of the CMUT array were first wirebonded to a secondary PCB which was connected to beamformer PCB with pin header. The CMUT array was coated with 3 μm Parylene C to isolate the electrical connections in water. Due to limited number of channels on the test beamformer, only 16 CMUT array element were used in the experiment. A Petri dish was placed enclosing the CMUT array to be used as a water tank for the experiments. A hydrophone (HNA-0085, Onda Crop., Sunnyvale, CA) was used to measure the 2-D transmitted pressure fields. For this purpose, the hydrophone was mounted on a XYZ stage connected to three linear actuators which were controlled by a motion controller (ESP 300, Newport Co., Irvine, CA).

First the beamformer was programmed with pulse width values of 70 ns. Focused beams were generated and were captured with the hydrophone under immersion. Figure 2.14(a) shows the captured hydrophone signal and Figure 2.14(b) shows the corresponding frequency responses of the captured signal.

The CMUT elements were excited from the integrated pulsers with a 30 V unipolar pulse and a pulse width of 60 ns without applying any bias voltage. First a non-steered plane wave was generated and a horizontal 1-D scan with the hydrophone was performed to determine the center point of the scan by finding the maximum pressure location. Then, a raster 2-D scan on XZ plane was performed starting from the bottom corner. The hydrophone was stepped in 100 μm increments to form a 6 mm $\times$ 6 mm plane using 3721 measurement points. Each point of pressure data for a particular scan location was averaged and captured by a PC. The data was further

processed to find the peak-to-peak pressure values for each raster point.

Three different beam profiles were generated to demonstrate the functionality of the beamformer. The focal point for the focused beams both in steered and non-steered cases was 4 mm and the steering angle was 25 degrees for the steered beam. Simulated beam patterns were also calculated for the same array structure using Field II and plotted together with the measured beam patterns in Figure 2.15. All beam pattern plots were normalized to each of their maximum. The measured beam patterns show close match with the simulated results up to -10 dB. The discrepancy between two plots especially on larger angles from the normal of the array is mostly due to decrease in the sensitivity of the hydrophone for large acceptance angle and non-uniformity of the array elements. The focal points in the beam pattern plots were observed as slightly closer than the actual focal distance because of the delay quantization errors due to clock resolution of the system and possibly a tilt on the raster scan plane in elevation direction.

CHAPTER 3

ANALOG FRONT-END CIRCUIT

3.1 Analog Front-End (AFE)

To measure ultrasound echo signals from CMUTs, a Low-Noise-Amplifier (LNA) was designed. The front AFE was designed to have bandpass characteristics with low cutoff frequency of 0.9 MHz, high cut-off frequency of 12.5 MHz and mid-band closed loop gain of $\approx$ 14.5dB. The bandpass response of the front-end amplifier helps reduce aliasing and noise folding due to TDM in the later stage. Figure 3.2 shows the architecture of the implemented AFE. A telescopic op-amp with simulated open loop gain of $\approx$ 60dB was implemented as the core amplifier. The small-signal analysis yields the transfer function of the AFE is given by

$$H(s) = 1 + \frac{\frac{R_f}{1+sR_fC_f}}{\frac{\frac{1+sR_iC_i}{sC_i}}} \tag{3.1}$$

$$H(s) = \frac{1 + s(R_iC_i + R_fC_i + R_fC_f) + s^2(R_iC_iR_fC_f)}{(1 + sR_iC_i)(1 + sR_fC_f)}$$

The choice of R_i, R_f, C_i, C_f is such that $R_iC_i + R_fC_i + R_fC_f \gg R_iC_iR_fC_f$ and $R_iC_i + R_fC_i \gg R_fC_f$. Then

$$H(s) \approx \frac{1 + sC_i(R_i + R_f)}{(1 + sR_iC_i)(1 + sR_fC_f)} \tag{3.2}$$

The dominant LHP zero is given by

$$f_{Z1} = \frac{1}{2\pi C_i(R_i + R_f)} \tag{3.3}$$

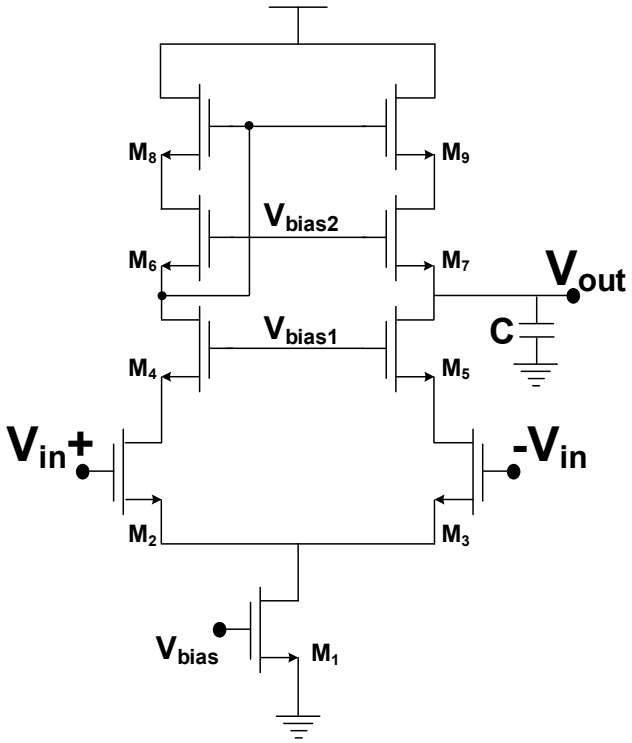

Figure 3.1: Schematic of the op-amp.

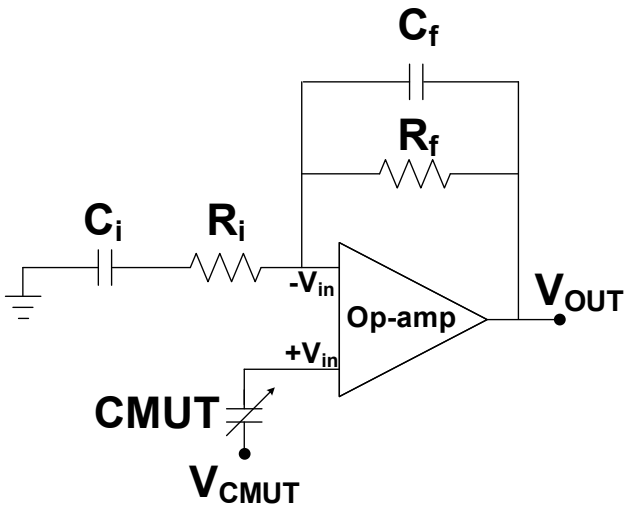

Figure 3.2: Architecture of the implemented Analog Front-end amplifier.

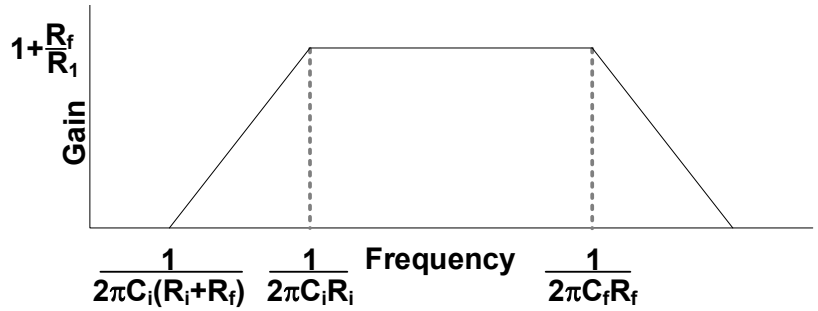

Figure 3.3: Theoretical magnitude plot of the implemented Analog Front-end amplifier.

The LHP poles are given by

$$f_l = \frac{1}{2\pi C_i R_i} \tag{3.4}$$

and

$$f_h = \frac{1}{2\pi C_f R_f} \tag{3.5}$$

f_l sets the lower cut-off and f_h sets the higher cut-off frequencies of the front-end amplifier. The mid-band gain is set by R_i and R_f and is given by

$$A = 1 + \frac{R_f}{R_i} \tag{3.6}$$

Figure 3.3 shows theoretical magnitude plot of the implemented AEF.

The input-referred spectral density of the noise of the designed AFE can be adopted from [49] as

$$e_i = \sqrt{\frac{ENBW * 4kTR_f}{A} + {e_\omega}^2(f_{enc} ln \frac{f_h}{f_l} + ENBW)} \tag{3.7}$$

Where, f_{enc} and e_ω are voltage noise corner frequency and voltage white noise spectrum that dominates core op-amps noise density. f_l and f_h are lower and higher

cut-off frequencies shown in shown in equation 3.4 and 3.5 respectively. A is the closed loop gain shown in equation 3.6 ENBW is the effective noise bandwidth and for single pole band-pass amplifier

$$ENBW = \frac{\pi}{2}(f_h - f_l) \tag{3.8}$$

From equation 3.7 it can be seen that, for a fixed closed loop gain the input referred noise has a proportional relationship with the value of feedback resistor R_f. The noise can be reduced by lowering the value of R_f, but to keep the gain constant the value of R_i would also needs to be lowered. Lowering the value of R_f and R_i causes higher power consumption. The noise level can be significantly improved with a more relaxed power requirement, which enables decreasing the values of R_f and R_i. To verify the functionality of the designed AFE with a output buffer circuit was fabricated on the die for test purpose. To measure the frequency response a sinusoidal signal was provided from a Agilent 81150A signal generator to the input of the amplifier. The input signals frequency was swiped from 1 MHz to 20 MHz. Output of the amplifier was measured. To get accurate results the output buffer was also characterized for the frequency range. Then the voltage gain of the amplifier was divided by the buffer gain to extract amplifier gain. The measured and simulated frequency response of the test AFE is given in Figure 3.4. Device parameter of the AFE is given in Table 3.1

For noise measurement of the AFE, the output of the test amplifier was connected to an Agilent 4395A spectrum analyzer in spectrum analyzer mode. The input noise spectrum was obtained by dividing the measured output noise with the gain of the output buffer and the amplifier.

Figure 3.5 shows the simulated and measured input referred noise of the front-end amplifier. The total input noise of the amplifier can be obtained by integrating measured input referred noise spectrum over the ENBW and was calculated to be

Table 3.1: DEVICE PARAMETERS OF THE AFE

Parameter	**Value**
M_1, M_2-M_3, M_4-M_5	32/0.25, 24/0.25, 20/0.25 (NMOS)
M_6-M_7, M_8-M_9	20/0.25, 50/0.25 (PMOS)
C_L, C_i & C_f	0.5 pF, 30 pF & 0.4 pF
R_i & R_f	4 kΩ & 24 kΩ
Mid-band Gain, f_l & f_h	≈ 14.88dB, 700 kHz & 12.4 MHz (Measured)
Input refereed noise	≈ 60 μV (Measured)
Power	50 μW for 10% duty cycle (simulated)

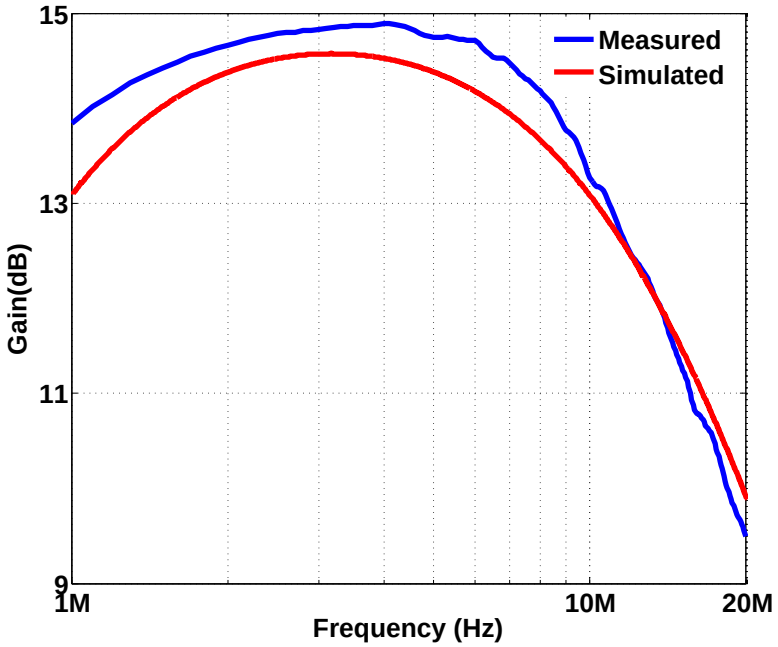

Figure 3.4: Frequency response of the test analog front-end amplifier.

≈ 70μV. The simulated total noise of the fabricated CMUT was ≈ 90μV. The input amplifier was intentionally designed to have lower noise figure than the CMUT to have better system performance. Simulated CMUT noise and measured input referred noise of the AFE is shown in Figure 3.6.

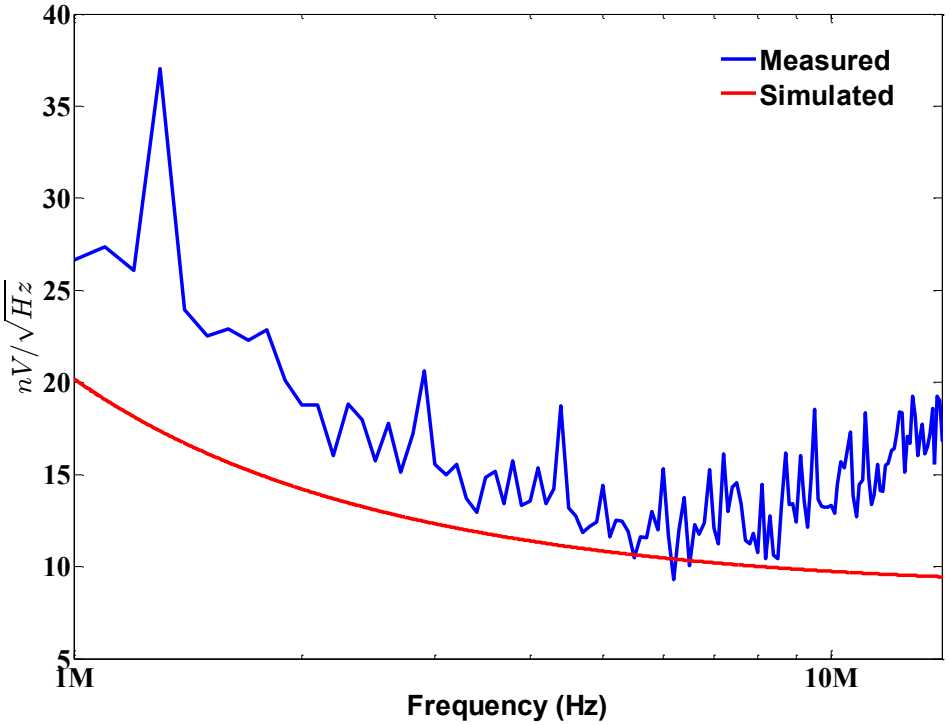

Figure 3.5: Measured (blue) and simulated (red) input noise spectrum of the front-end amplifier.

3.2 Time Gain Control (TGC) Circuit

The next stage of the chain is a 4 level TGC circuit to improve the dynamic range of the system by up to 12dB. The schematic of the implemented TGC circuit is shown in Figure 3.7(a). The gain of the TGC circuit is controlled by opening and closing the transmission gate a, b & c switches. At the lowest gain stage, all the switches are kept closed and the gain of the circuit becomes $-\frac{R_{ft}}{R_{it}}$. To increase the gain of the first switch a is opened and the feedback resistance value increases and the gain doubles. To achieve higher gain switches b and c can opened. A 2-bit digital counter and a 2 to 4-bit decoder was implemented to send control signal to the gate of the gain controlling switches. The timing of the gain control signal can be sent from outside from the FPGA via same μ-coax cable which will be used to program the

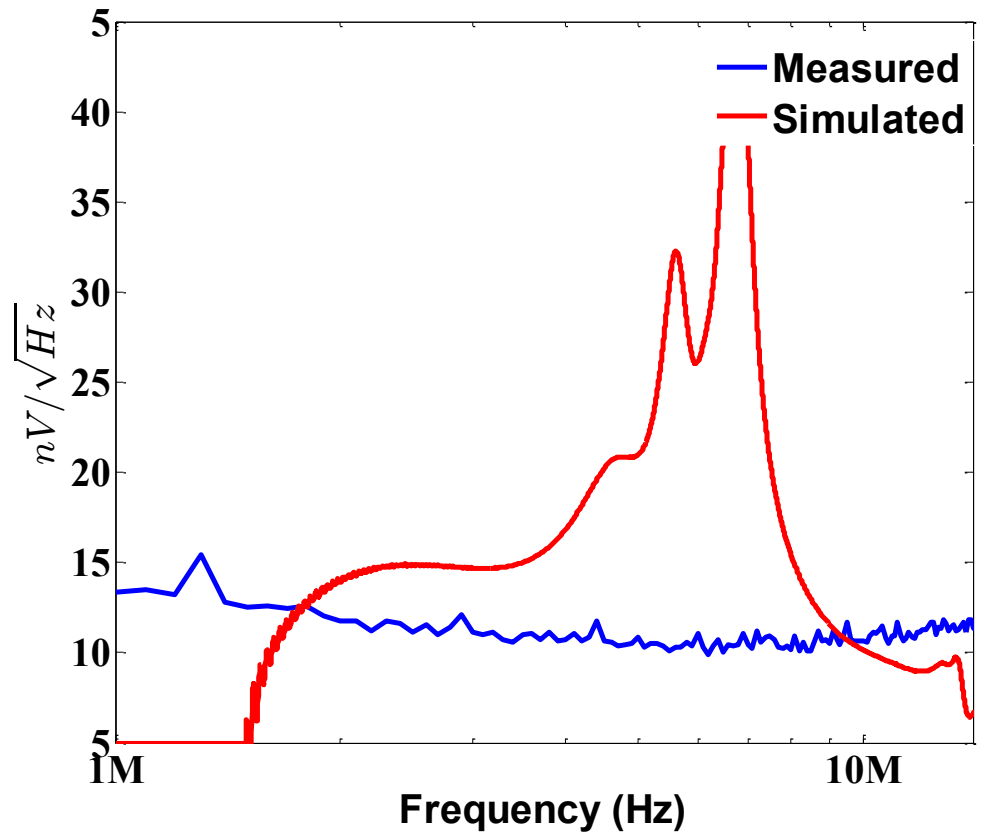

Figure 3.6: The blue curve shows measured input referred noise spectrum of the AFE amplifier and red curve shows simulated noise spectrum of CMUT.

transmitter beamformer. During the data load mode of the transmit beamformer, the 2-bit counter of the TGC controller can be kept on Reset mode. Once the data loading of the transmitter beamformer is complete the reset signal of TGC control counter can be de-asserted. During the receive mode pulses can be sent via **Data_In** cable to change the gain state of the TGC circuit. To verify the functionality of the TGC a test circuit was implemented on the die. A 7 MHz monotone sine-wave was feed to the input. The gain was varied and the output was captured using Agilent MSO7104A oscilloscope. Figure 3.7(b) shows measured transient response of the TGC circuit.

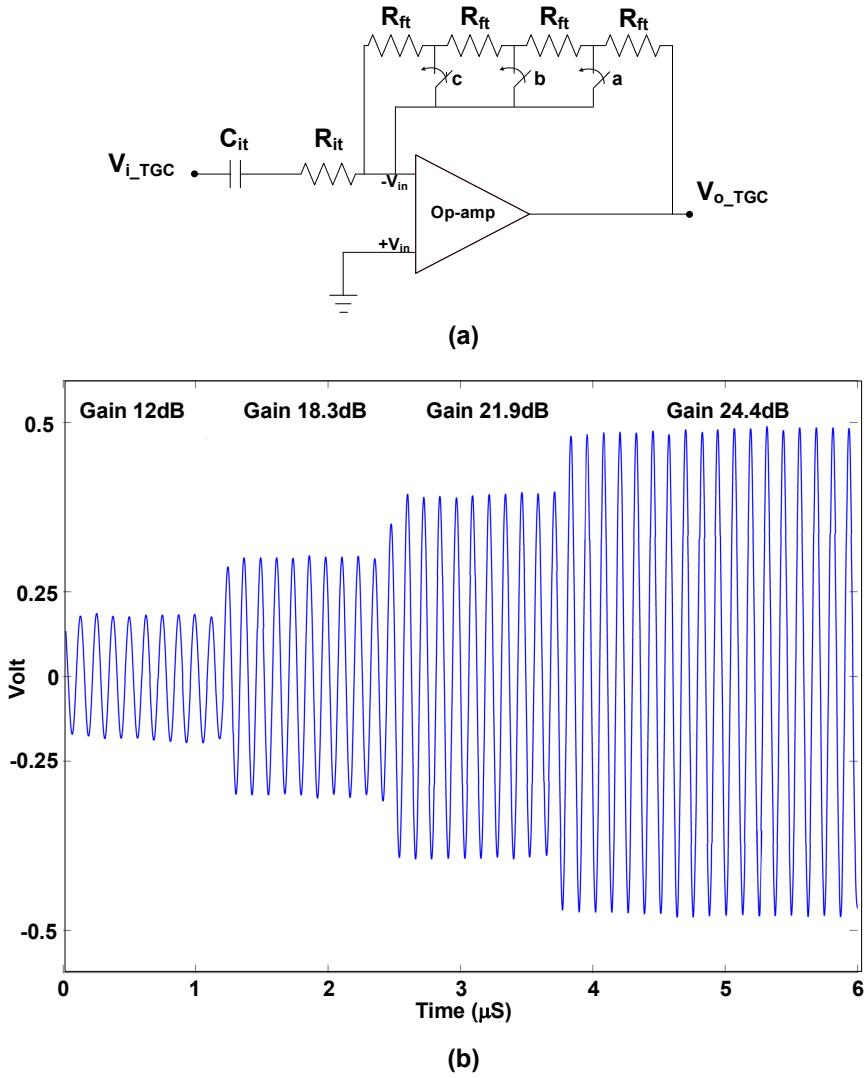

Figure 3.7: (a)Schematic of the implemented TGC circuit (b) Measured transient response of the TGC circuit.

CHAPTER 4
RECEIVE SIGNAL MODULATION TECHNIQUES

In order to reduce the receiver cable count, the receiver channels need to be multiplexed. Digital modulation will require A/D converters for each channel which are power hungry, and will consume significant area and thus is not suitable. Therefore, analog modulation is more promising for channel multiplexing. In this chapter, first we explore analog orthogonal FDM method (OFDM), We then introduce the custom designed receiver front-end with OFDM chip and discuss its main building blocks in detail. We present the post layout simulation results as well as numerical demodulation which show the theoretical viability of the approach. Test results of some of the building blocks are also presented. We also discuss some practical limitation of implementing analog OFDM circuit in an area and power restricted application such as ICE. In later part of this chapter we also explore analog Time Division Multiplexing (TDM) approach which is a much simpler and practical approach for receiver cable reduction.

4.1 Analog Frequency Division Multiplexing (FDM)

Utilizing analog Frequency Division Multiplexing (FDM), outputs of the CMUT array elements can be shifted to higher frequencies. In addition, if orthogonal carriers are used then two CMUT outputs can be combined on a single carrier frequency [50]. Figure 4.1 shows the theoretical implementation of Orthogonal Frequency Division Multiplexing (OFDM). By choosing the appropriate carrier signals and band-pass filters (BPF) at the output of mixers the shifted signals can be combined without interfering with each other and sent out via a single cable. In this method, the message signals from consecutive channels are mixed with sine and cosine signals at

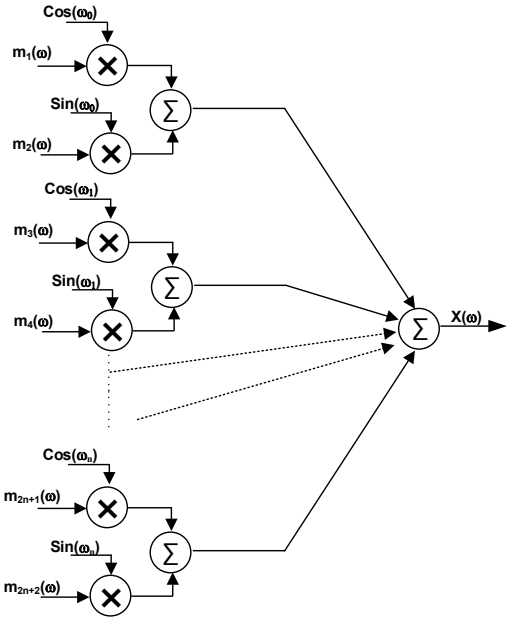

Figure 4.1: Block diagram of analog Orthogonal Frequency Division Multiplexing (OFDM).

a carrier frequency and added, with the final signal expressed as:

$$X(\omega) = \sum_{0,1,...k} m_{2n+1}(\omega) * cos(\omega_n) + m_{2n+2}(\omega) * sin(\omega_n) \tag{4.1}$$

For demodulation, the received signal is mixed with orthogonal sine and cosine signals at the modulation frequency and then low pass filtered to get back the message signals as:

$$X(\omega) * cos(\omega_n) \xrightarrow{LPF} m_{2n+1} \tag{4.2}$$

$$X(\omega) * sin(\omega_n) \xrightarrow{LPF} m_{2n+2} \tag{4.3}$$

4.1.1 8 Channel Analog OFDM IC

An integrated circuit was custom designed to multiplex the output of 8 CMUT array elements with center frequency 7 MHz and 80% fractional bandwidth for ICE application. Analog OFDM modulation with frequencies of 40 MHz, 80 MHz, 120 MHz and 160 MHz were chosen to provide enough separation between channels. The IC was designed in 0.35 μm 4M2P TSMC process with supply voltage of 3.3 V. Figure 4.2 shows the block diagram and layout of the circuit which consumes 0.7 mm $\times$ 1.76 mm area. The front end of the modulator consists of a low noise capacitive feedback TIA [51] with bandwidth of $\sim$20 MHz and gain of 87dBΩ. The output of the TIA was designed to be converted to fully differential and then feed to an anti-aliasing 4^{th} order biquad tunable gm-C low pass filter (LPF). To determine the order of the BPFs and to examine if the μ-coax cable and chosen ADC were compatible with the OFDM scheme, an experiment was conducted using Agilent Technologies 81150A Arbitrary Waveform Generator (AWG). In that experiment 7 MHz 80% bandwidth Gaussian pulses were multiplexed using 40 MHz, 80 MHz, 120 MHz and 160 MHz I/Q clocks using Matlab. The multiplexed data was uploaded to the AWG. The data form AWG was then captured with TIs ADC16DX370 device at 370 MHz via a μ-coax cable. From this experiment, it was found that in order to have acceptable amount of cross talk ($\sim$-40dBs) between the multiplexed signals at different bands, 8^{th} order BPFs were required. Figure 4.3(a) shows diagram of experimental setup and Figure 4.3(b) shows spectrum of the multiplexed signals after being filtered with 8^{th} order Butterworth BPFs.

4.1.2 Post Layout Simulation Results & Measurement Results

Before sending out for fabrication, a post layout simulation of the designed multiplexer circuit was performed in CADENCE using the Specter circuit simulation tool. In order to validate the performance of the analog OFDM and demodulation scheme

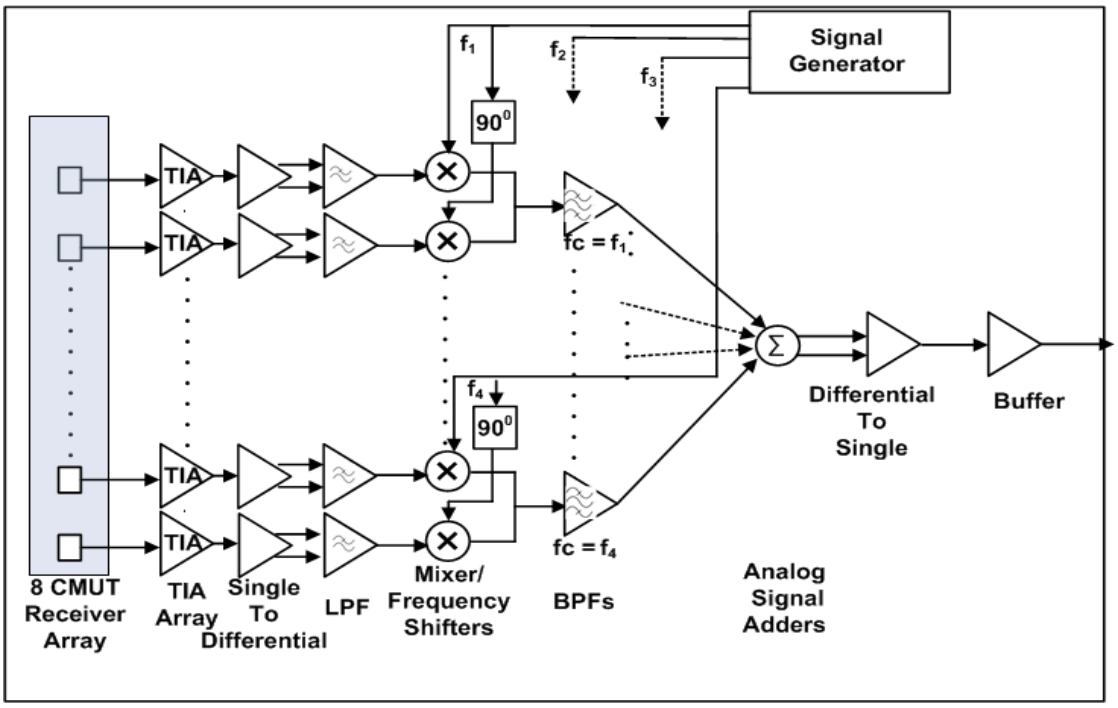

Figure 4.2: Block diagram of the implemented analog Orthogonal Frequency Division Multiplexing circuit.

the chip was first simulated with two 7 MHz 80% bandwidth Gaussian pulses shown Figure 4.5(a). The two pulses were up-converted with orthogonal 40 MHz carriers shown Figure 4.5(b). The up-converted signals were then de-modulated to form the signals shown in Figure 4.5(c). It is clear from Figure 4.5(c) that relative amplitude and phase of the signals were preserved. Although not detrimental, cross talk between the channels, lower than -20dB, is also observed which due to the phase shift of the I/Q signal's modulator and demodulator clock. To verify the functionality of the entire designed chip 7 MHz 80% BW Gaussian pulses with different phase were applied to all 8 channels and modulated. The Figure 4.6(a) shows the frequency spectrum of a single channel input. Figure 4.6(b) shows the spectrum of two Gaussian pulses which are up-converted to 40 MHz, and Figure 4.6(c) shows the spectrum of all the up-converted signals.

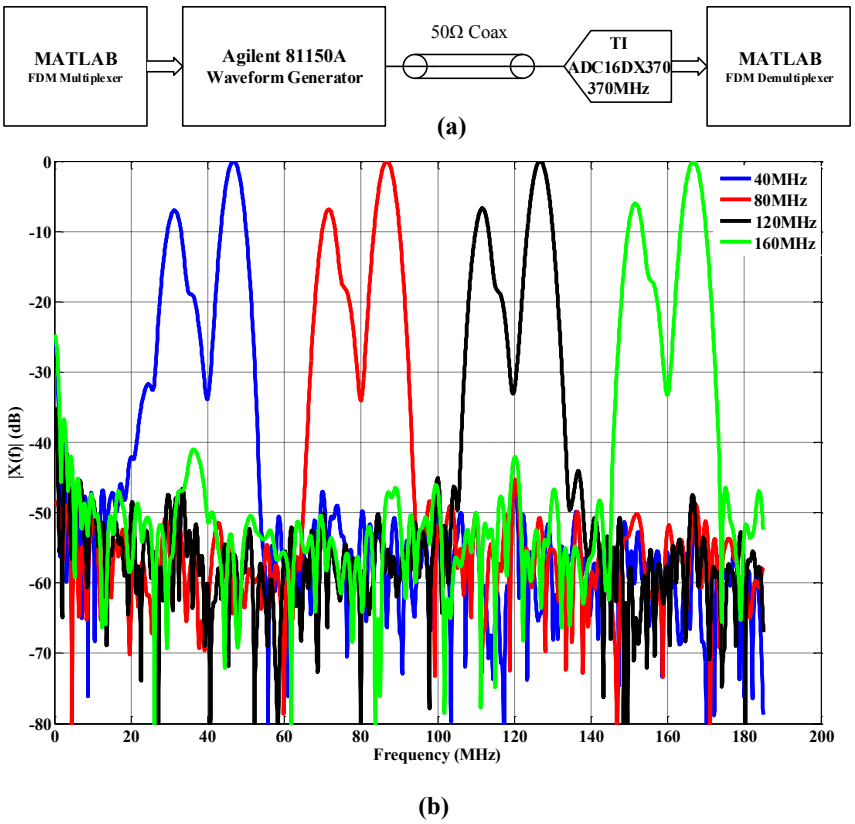

Figure 4.3: ((a)Block diagram of experimental setup (b)Spectrum of the multiplexed signals after being filtered with 8^{th} order Butterworth BPFs.

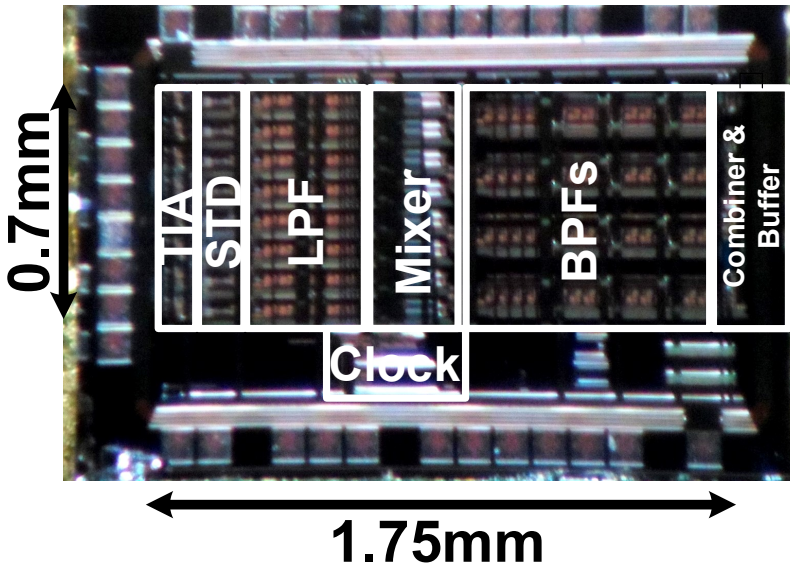

Figure 4.4: Micrograph of the fabricated IC of the Analog OFDM Modulator.

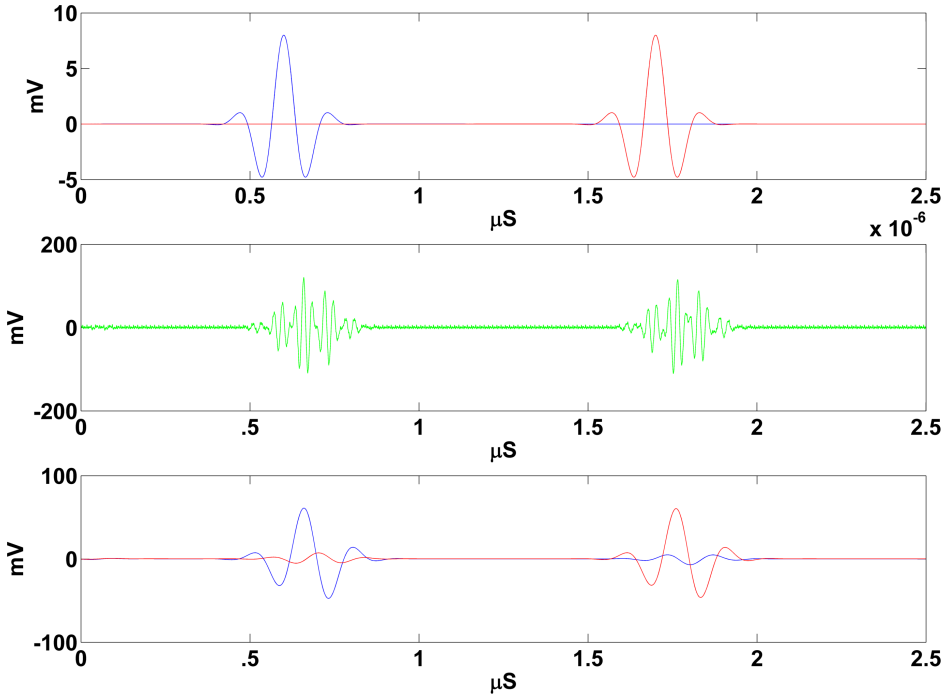

Figure 4.5: Transient simulation of Analog OFDM with 2 7 MHz Gaussian pulses.

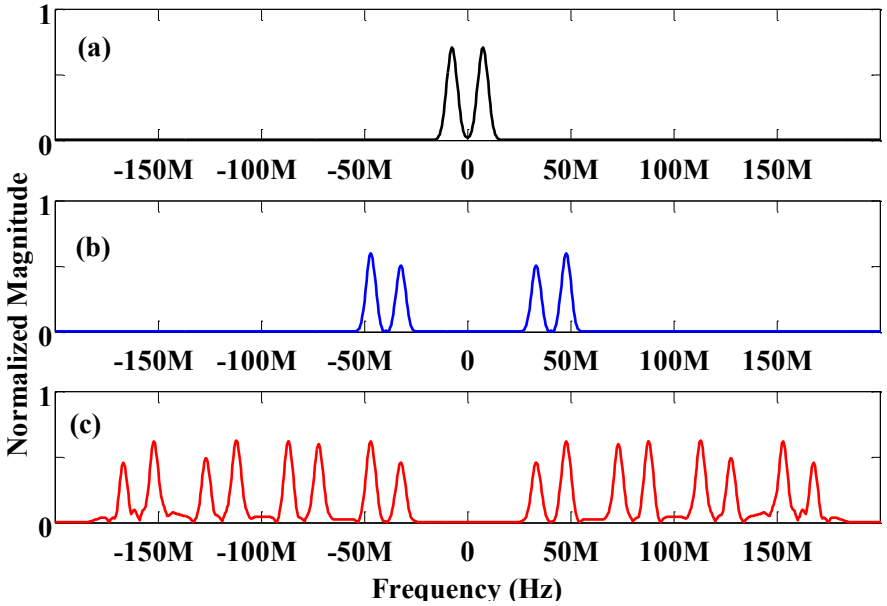

Figure 4.6: Simulated spectrum of 8 channel analog OFDM signals.

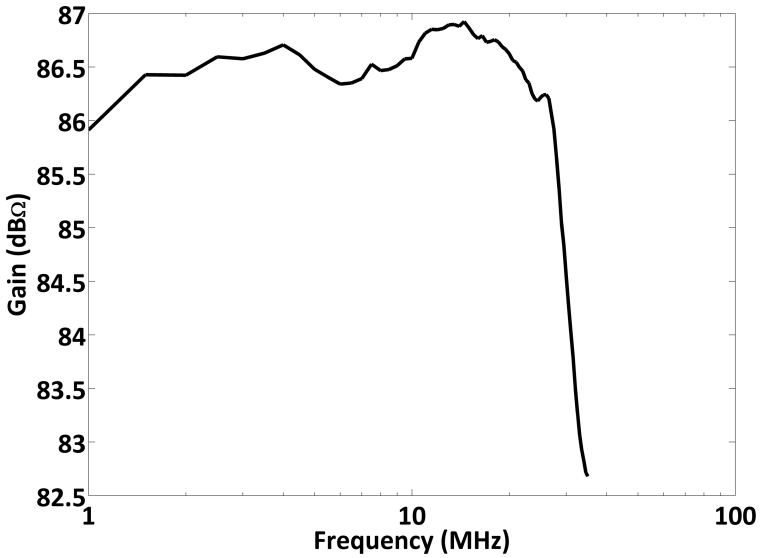

Figure 4.7: Frequency response of TIA.

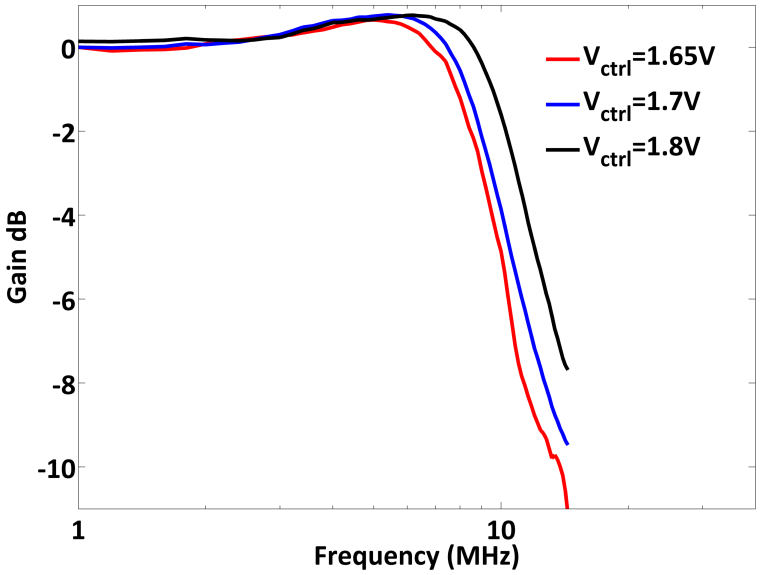

Figure 4.8: Frequency response of LPF.

4.1.3 Measurement Results

Each individual block of the fabricated chip was tested. Figure 4.7 shows the measured results for the TIA to have a gain of ∼86dBΩ and bandwidth of 20 MHz, as designed. The measured frequency response of the anti-aliasing tunable LPF is shown in Figure 4.8. The performance of on-chip orthogonal clock generator, single to differential convertor, mixer, combiner and output buffers performance was also verified.

The bandpass filter bank was found to be unstable as it is very challenging to design 8^{th} order gm-C bandpass filters phase margin within the power and area restrictions. These filters are extremely sensitive to silicon process variations and would require a tuning mechanism for each individual filter - this may not be feasible to implement in a high density imaging catheter system. Also, any phase shift between the I/Q clock signals shall result in cross talk. Furthermore, complex hardwire and software would be required for demodulating the OFDM signals in a real-time imaging system.

4.2 Time Division Multiplexing

Time-Division Multiplexing (TDM) has been used extensively in communications systems to reduce the number of channels [52, 53, 54]. With proper design, it can be used for ultrasound applications. This approach allows multiple channels to share the same cable by assigning each channel a time slot in which to transmit. Analog TDM requires a relatively small amount of hardware and power as it requires only an analog multiplexer and digital counting logic to multiplex analog data. This could make it suitable for catheter based ICE application. In this approach, the multiplexer scans through every element in turn using a sampling clock which is at least n times the Nyquist rate (where n is the number of channels). This approach was briefly expressed in [55] in which 12 channels were multiplexed onto a single cable using this technique. The approach has since been demonstrated in [56] and [57] in which 8:1 and 4:1 reduction in cable counts were achieved respectively.

This research focuses on the design of low noise analog front-end (AFE) electronics for CMUTs along with TDM electronics which would be located with the transducer to reduce the number of cable coming out of the catheter. Also, this research shall make use of Direct Digital Demutiplexed (DDD) technique [55, 58] and describe the implementation of transducer side electronics for the utilizing the DDD method. Using the DDD scheme the output data of the TDM can directly be feed to an ADC

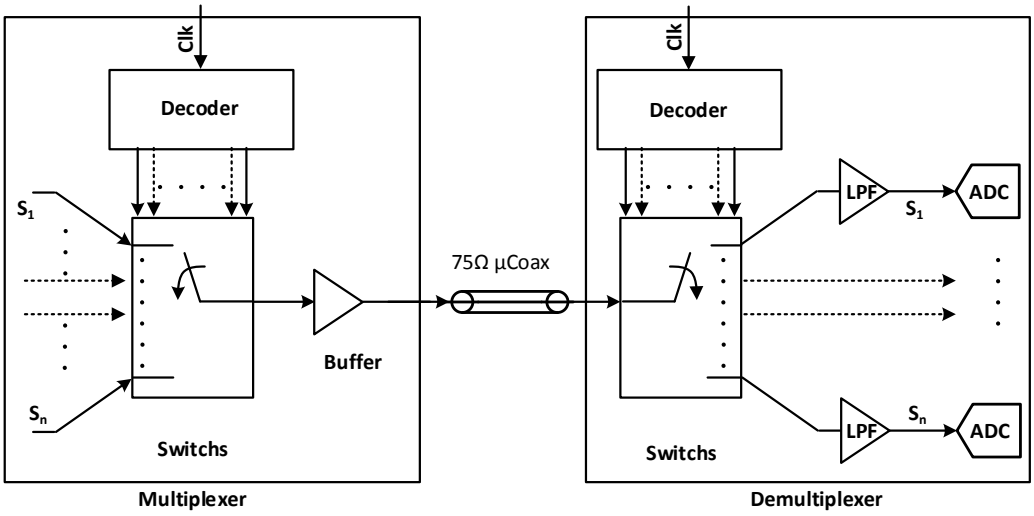

Figure 4.9: Block Diagram of standard Time Division Multiplexing and Demultiplexing scheme.

which will be running at same frequency as the TDM. In the DDD method the system can be designed such that each ADC sample corresponds exactly to one channel in the multiplexed data. This means that as the samples are taken, demultiplexing becomes a simple task of separating the data into groups consisting of every n^{th} sample. This results in a data stream for each TDM channel which can each then be filtered and interpolated using DSP techniques. DDD eliminates the need for analog domain demultiplexing, resulting in both removal of the analog switches and filters and reduces number of ADCs required for the standard design. The detail description of DDD can be found in [55, 58].

In Figure 4.10 an overview of the simplified 8 channel TDM scheme is shown with DDD technique. To send 8 CMUT signals with center frequency of 7 MHz 80% bandwidth via single cable the clock frequency of the multiplexer needs to be 156.8 MHz or higher to satisfy the Nyquist sampling requirement. If the clock frequency is set to 200 MHz then the sampling frequency for each channel, will be 25 MSPS. The sampled analog signal pulses need to reach steady state fast enough so that the

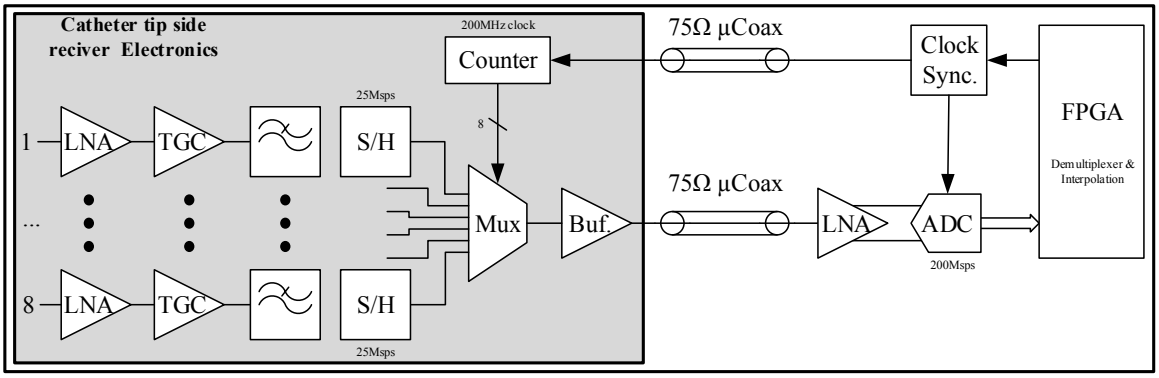

Figure 4.10: Block Diagam of Analog Time-Division Multiplexing Scheme using Dirict Digital Demultiplexing.

external ADC can sample the amplitude correctly. For the mentioned 8 channel TDM chip sampling rate per channel is 25 MSPS or 200 MSPS for all the channels, to limit the amount of cross-talk between the adjacent channel of the TDM signals the buffer driving the 75Ω cable and the cable needs to have at least bandwidth of 400 MHz. At the receiving end, the TDM signals are amplified with high speed LNA then digitized with a high speed ADC that is running at same speed as the TDM.

A key part of the DDD is the synchronization required between the TDM multiplexer and the sampler of the ADC. Before multiplexing the CMUT signals link training needs to be performed to synchronize the ADC with TDM. During the link training period transducer side electronics generate a proper training sequence. In the training sequence, channel 1 is connected to a fixed value voltage level V_{DC1} while other channels are connected to another value voltage level V_{DC2}. Figure 4.11(a) shows the configuration of the TDM during link training. By analyzing the TDM data during link training, it is possible to identify from the receiver side which is channel 1and properly phase align the TDM and ADC clock as there will be significant difference between one sample than the others.

Once phase alignment is complete all the channel is connected back to the corresponding AFE for data collection as shown in Figure 4.11(b).

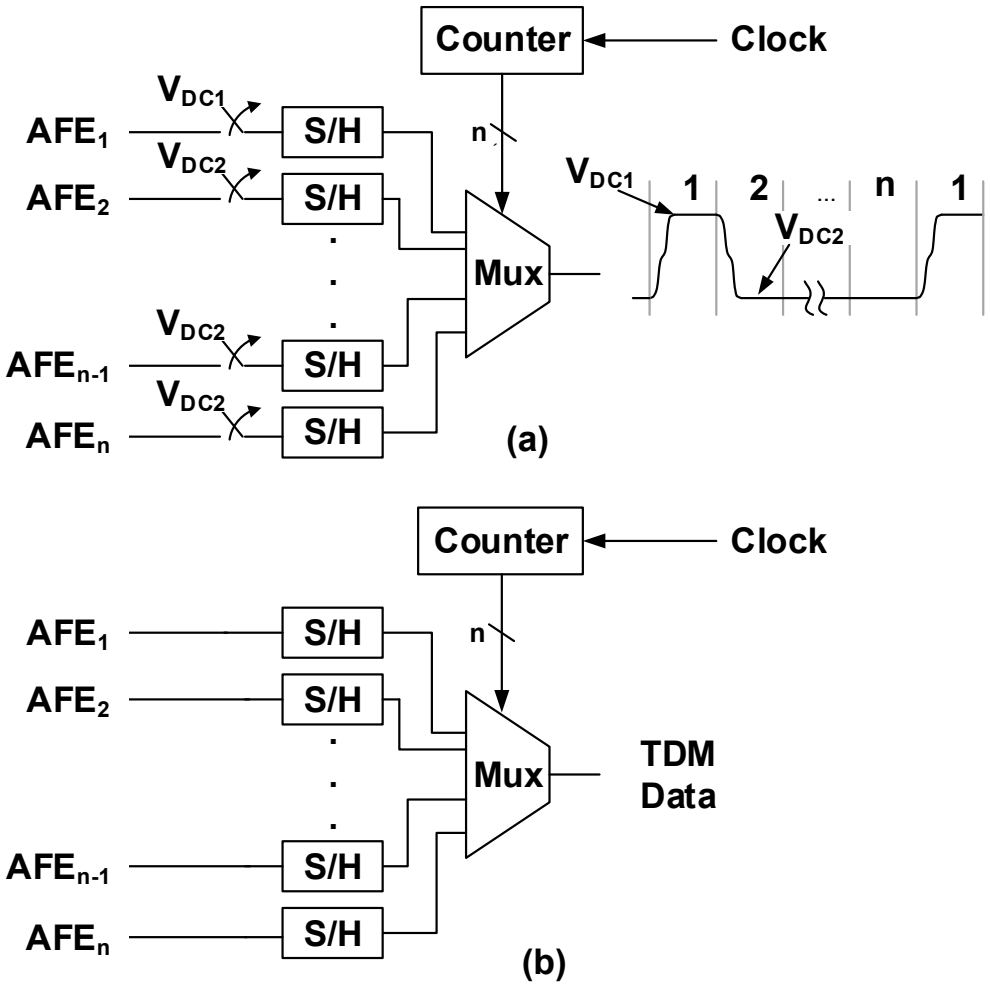

Figure 4.11: (a) TDM configuration during link training Period. (b) TDM configuration during normal operation.

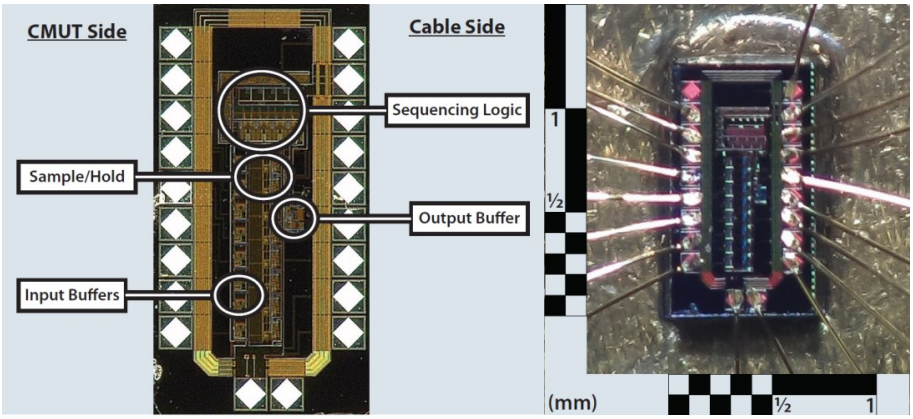

Figure 4.12: Micrograph of the designed prototype 8×1 TDM IC (active area .80 mm × .26 mm).

4.2.1 Prototype TDM IC Design

To verify the TDM scheme along with DDD a prototype TDM multiplexer stage for 8 input channels, comprised of four 8×1 multiplexers, has been fabricated in 0.35 μm 2P4M TSMC process and operates from a 3.3 V supply. The implemented circuitry, shown in Figure 4.12, occupies an area of 0.80 mm × 0.26 mm (without the bond pads). The chip consumes on average of 3.9 mW power, assuming a 10% duty cycle on time. The circuitry was designed to run at 200 MHz, sampling each channel at 25 MSPS. Furthermore, as it was designed solely for testing the TDM scheme only, there is no AFE present in the design. Instead the input stage is a unity gain buffer.

The input buffer drives the signal into the S/H capacitor via a pass transistor which allows the input to be sampled when connected, and then disconnected to hold the value ready to be multiplexed. Each buffer also has a controllable resistor, either pull-up or pull-down, which are enabled when the sequencing logic is switching into link training mode in order to generate the required pulse sequence. A digital counter is implemented which generates control signals for the switches for each hold capacitor to sequence selection of each channel by the analog multiplexer. The final output stage is a current feedback buffer adopted from [59] which has an output bandwidth of 450 MHz when driving a 75Ω||15 pF load.

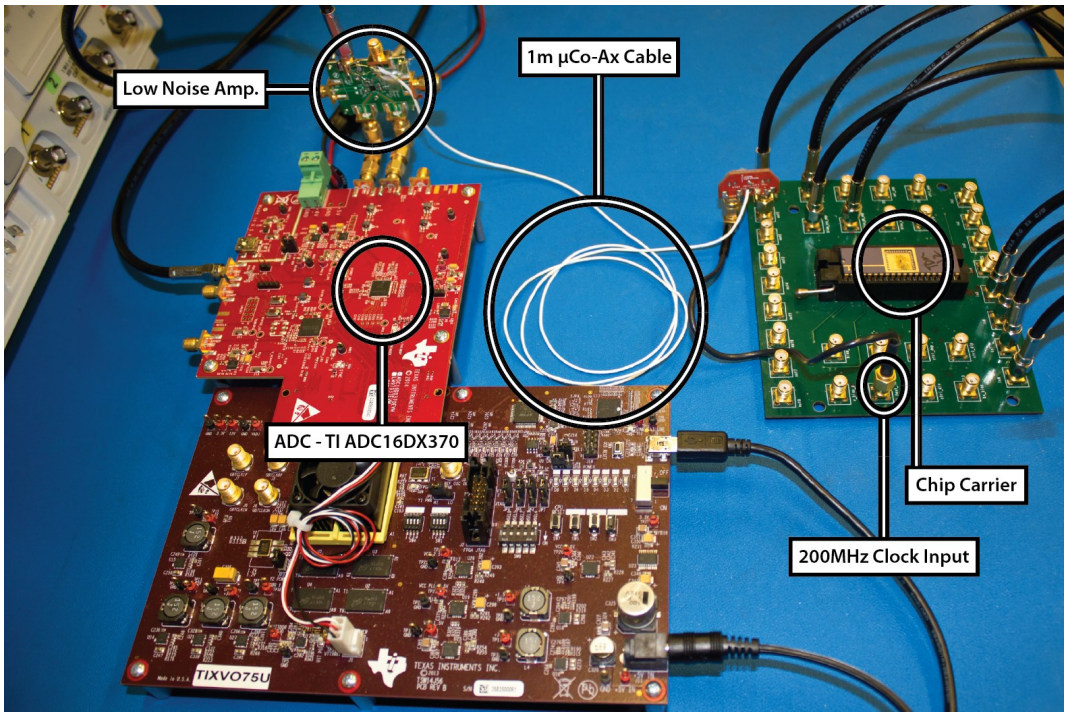

Figure 4.13: Experimental setup for testing the TDM multiplexing and data digitizing.

4.2.2 Initial Experimental Results

The fabricated silicon was diced and wire bonded to a chip carrier and then connected to a PCB to properly power and bias the circuit. The output of the multiplexer was connected to a 1m length of 48 AWG μ-coax cable with 0.17 mm outer diameter, as could be used in a catheter application, to ensure the results take into account the realistic effects of a bandwidth limited channel. Furthermore, as the TDM clock signal must also be routed to the multiplexer and may potentially present crosstalk issues, the clock in this experiment was fed through a μ-coax cable in the same bundle as the analog signal.

At the receiving end, the TDM signal was amplified using Texas Instruments LMH5401 LNA. This amplifier provides a close loop 12dB voltage gain. To reduce the crosstalk among the channels due to reflection issue the input of the LNA was properly matched with the cable. The amplifier converts the single ended input to differential output and was connected directly to the input of a high speed ADC on

a TI ADC16DX370EVM board.

The data from ADC was captured using a FPGA and transferred to the PC via USB. The link training was performed by manually adjusting the phase between the ADC and TDM clocks. The data from ADC was processed using a FPGA simulation. In the future Stratix V GS FPGA shall be used for real time data processing and link training.

Using the fabricated IC, the concept of the Direct Digital Demodulation technique was verified and also the amount of crosstalk shall between the channels as a result of multiplexing was determined.

A 200 MHz clock signal was used for both the TDM and ADC. The frequency was chosen as a trade-off between sampling rate and the bandwidth requirements of the cable. To determine the crosstalk among the channels, a 7 MHz sine signal was given as input to channel 1 and other inputs were connected to a DC bias. Figure 4.14 and 4.15 show the recovered signal for the case of a 7 MHz monotone, both in the time and frequency domain the results are from the output of the FPGA simulation, which after the interpolation and decimation performed by the FPGA, are sampled at 50 MSPS. As seen from Figure 4.14, the tone has clearly been recovered in the demultiplexing process, with the FFT of the signal showing a clear spike at 7 MHz. There is some crosstalk occurring between channels as evidenced by the 7 MHz spike on the other channels which should have no signal. The level of the crosstalk signals is less than -40dB when compared to the signal on channel 1. It should be noted that this is a measurement of the crosstalk between signals in the same μ-coax cable as a result of the multiplexing scheme. The electrical crosstalk between the two separate μ-coax cables in a catheter bundle was measured to be below -60dB at frequencies up to 600 MHz, therefore it is the TDM crosstalk which represents the limiting factor in this scheme. After the 7 MHz monotone experiment a sinc pulse with approximate bandwidth of 11 MHz was provided as input of channel 1 and others were connected

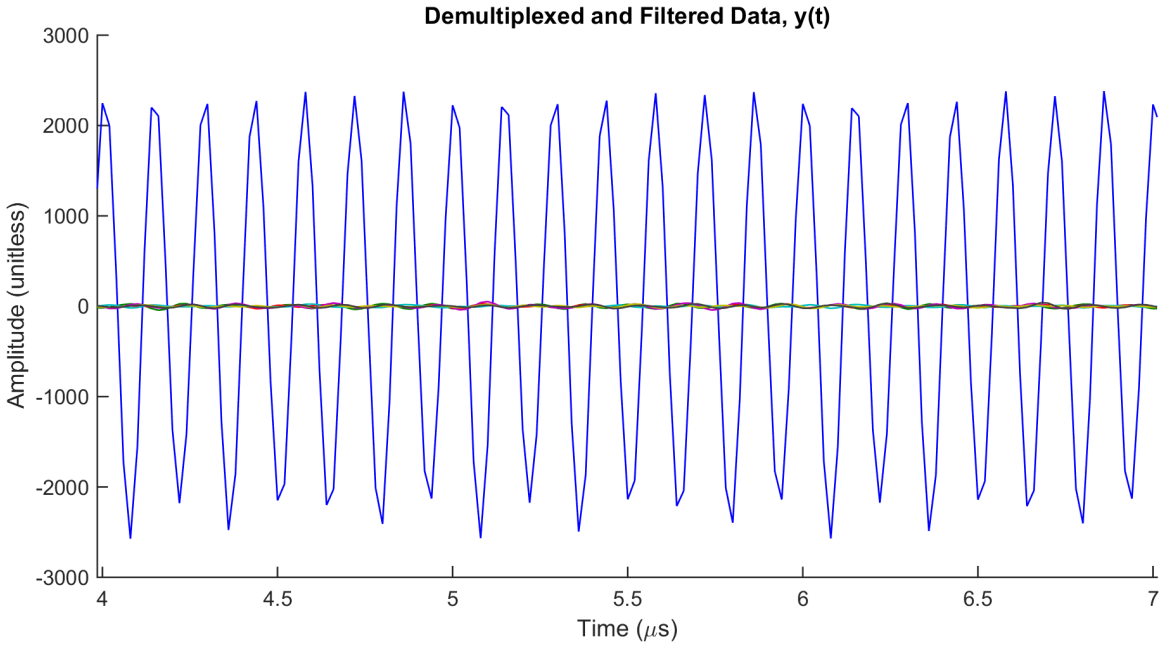

Figure 4.14: 7 MHz tone demultiplexed from TDM and interpolated to 50 MSPS.

to DC bias. The sinc pulse more realistically resembles an ultrasound pulse for ICE application. Observing the signal recovered from feeding in a sinc pulse, Figure 4.16, the signal has also clearly been recovered correctly, with a fairly flat response across the pass band of the spectrum. The signals are band-pass filtered in the FPGA with cut-off frequencies of 3 MHz and 10 MHz resulting in the relatively empty spectrum outside this band. It is difficult to determine from the frequency domain what level of crosstalk is present between channels, however by measuring the peaks in the time domain, this crosstalk is roughly -36dB similar levels to the tone test. Figure 4.17 shows the frequency spectrum of the recovered sinc pulse. Experimental results of the fabricated multiplexer in CMOS 0.35 μm process coupled with a 1 meter length of narrow diameter μ-coax cable and a high-speed ADC, shows TDM technique with DDD is suited for ultrasound catheters. The detail description of TDM technique with DDD and the fabricated IC has been reported in [58].

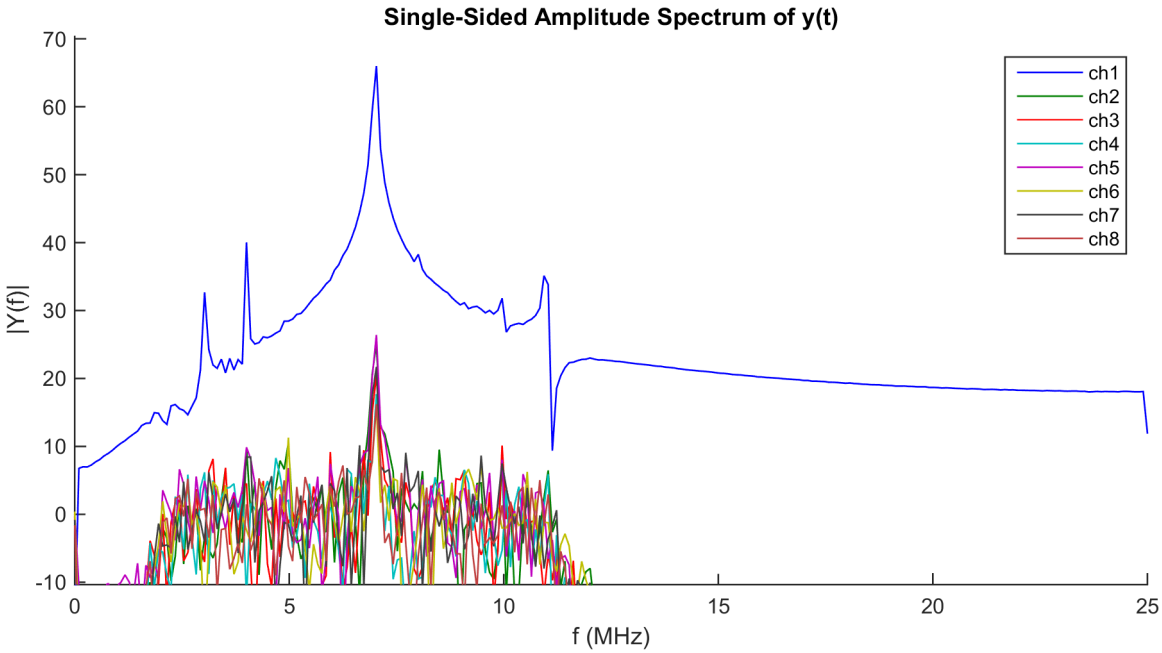

Figure 4.15: FFT of 7 MHz tone showing crosstalk levels.

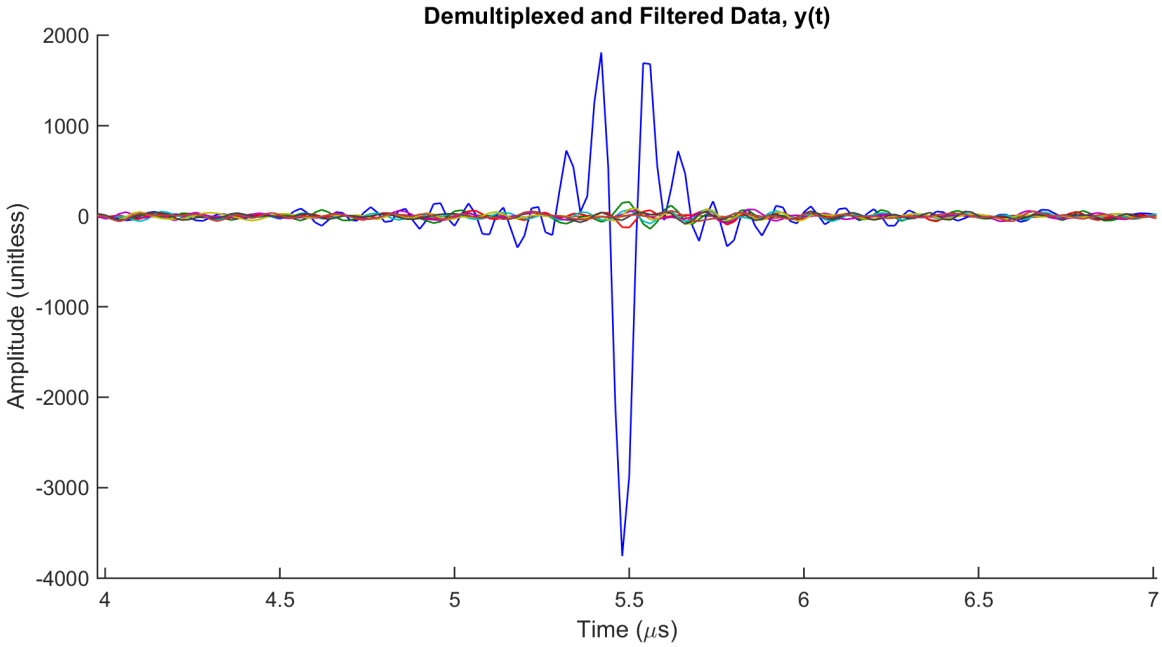

Figure 4.16: Sinc pulse demultiplexed from TDM.

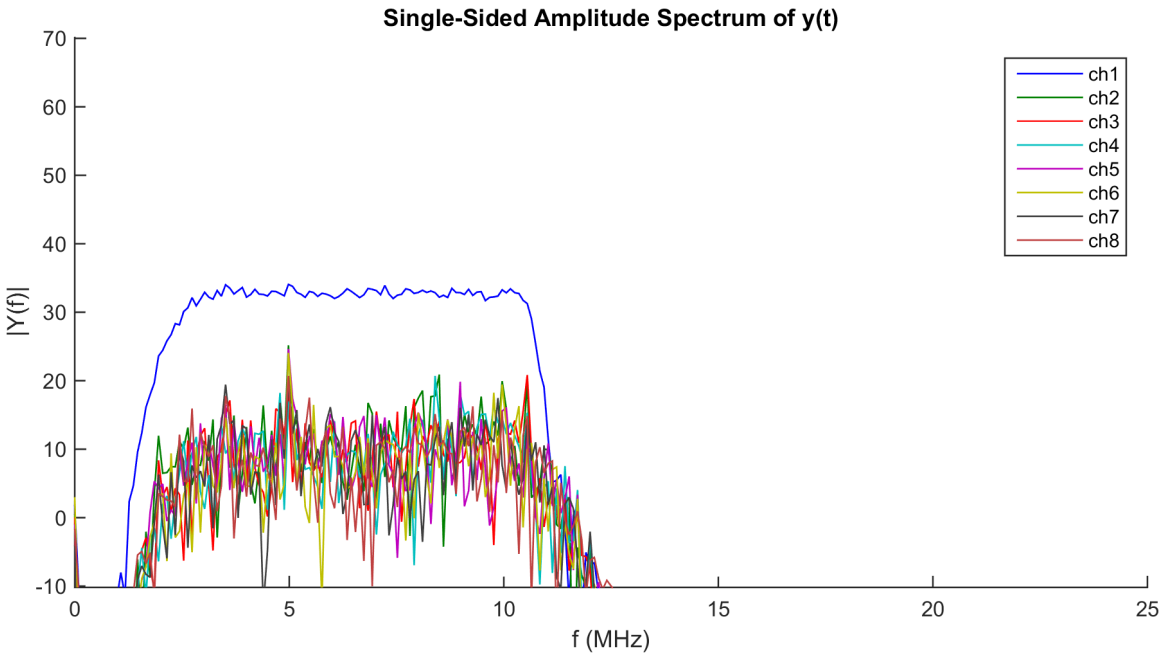

Figure 4.17: FFT of the demultiplexed Sinc pulse signal.

CHAPTER 5
IMAGING SYSTEM WITH TRANSMITTER AND RECEIVER CABLE REDUCTION TECHNIQUE

The main objective of this research work is to find an engineering solution for cable reduction for high density ultrasound imaging array. In the previous chapters, we first introduced an area efficient transmit beamformer circuit design which can be programmed via a single μ-coax data cable to produce desired ultrasound beam patterns. We then described the details of the beamformer system and the high voltage pulser design. We presented detail electrical measurements on pulse width and delay control in addition to acoustic measurements obtained by the transmit beamformer when interfaced with a 1-D CMUT array with geometry and frequency response suitable for ICE. After describing the transmitter beamformer we briefly described the time division multiplexing (TDM) circuit to reduce receive cable count. In this chapter we present a prototype imaging system where massive cable reduction is shown by utilizing both the proposed transmitter beamformer and TDM receiver circuit. Block diagram of the implemented imaging system was shown in Figure 5.1. The prototype imaging system consists 32 receive channels and 16 transmit channels. The micro graph of the transmit beamformer is shown in Figure 2.10.

5.1 32 Channel Receiver Circuit

The receiver (RX) side of the design consists of a 32 channel. The receiver IC design implements a Low Noise Amplifier (LNA) based Analogue Front-End (AFE) with integrated Time Gain Compensation (TGC) coupled with analog Time Division Multiplexing (TDM) circuitry to achieve an 8:1 cable reduction. The RX IC operates from the same 1.8 V supply as the TX IC and consumes approximately 9 mW average

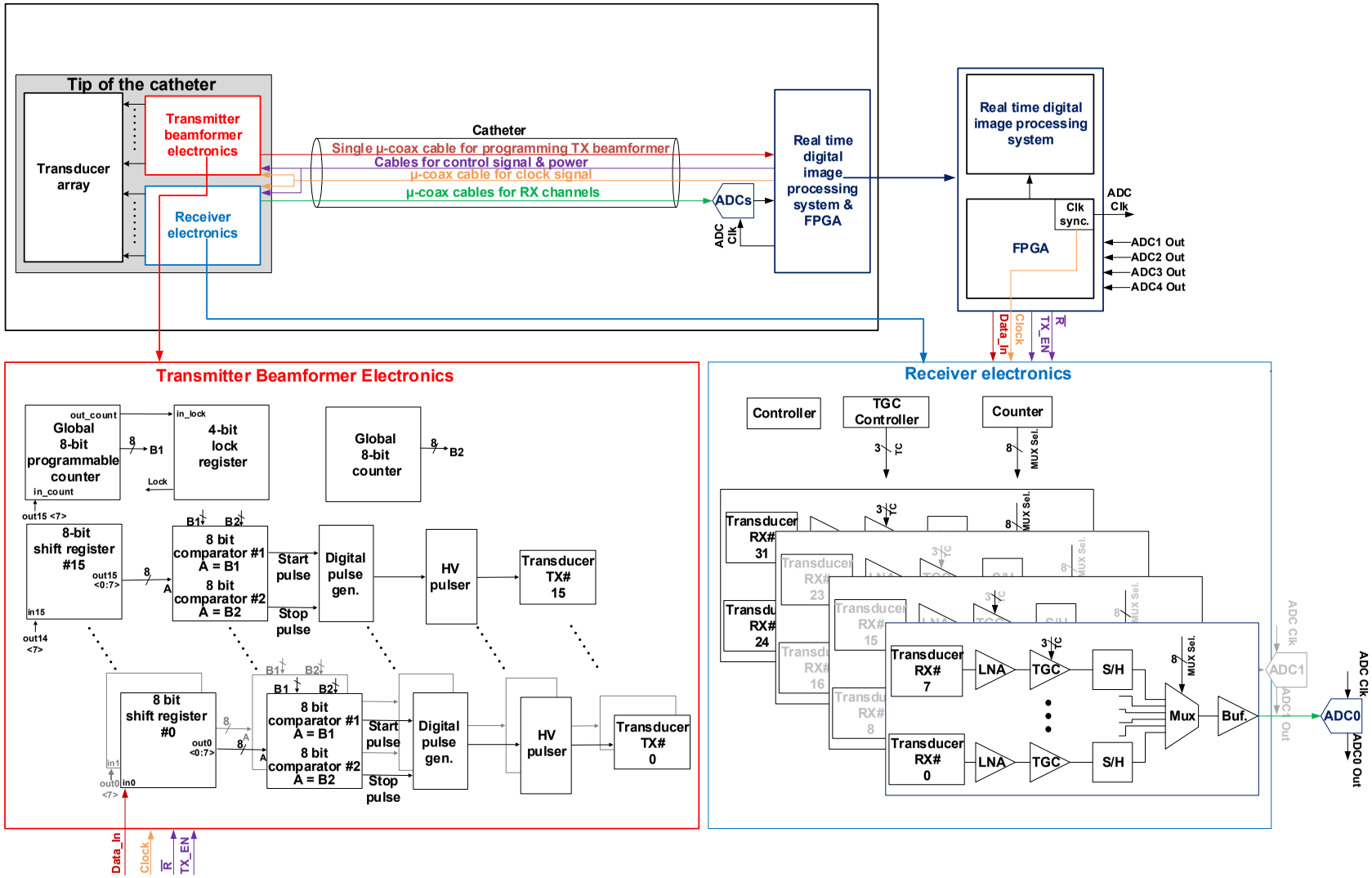

Figure 5.1: Block diagram of the proposed catheter based ultrasonic imaging system.

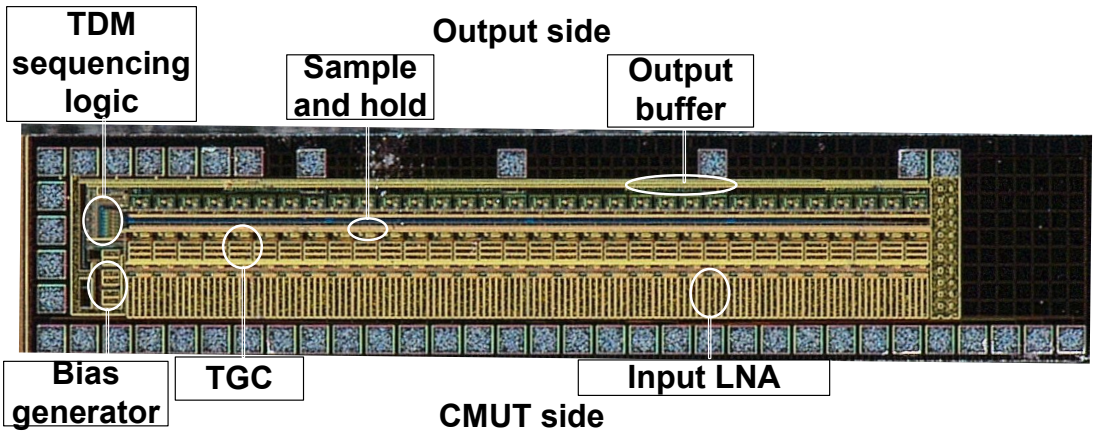

Figure 5.2: Micrograph of the receiver IC. Area 3.25 mm × 0.55 mm.

power (assuming a 10% duty cycle). The RX design requires 3.25 mm × 0.55 mm of IC area for the full 32 channel AFE and four 8×1 TDM multiplexers. The Receiver AFE was designed for 1-D element CMUT transducers with 7 MHz center frequency and 80% fractional bandwidth, and has been designed to have a 3-dB bandwidth of around 11 to 12 MHz. The amplified signals from the AFE were each sampled at 25 MSPS by the TDM front end, and then multiplexed into a TDM channel running at 200 MSPS utilizing the same clock as the TX IC. The receiver IC was fabricated using the same technology process as the TX IC. The micrograph of the RX IC is shown in Figure 5.2.

5.1.1 Time Division Multiplexing (TDM) & Buffer circuit

The final stage of the receiver chain is an 8×1 multiplexer and a high-speed buffer to drive μ-coax receiver cables. The multiplexer is used to reduce the number of connections from the receive transducer to the back-end electronics. The circuit consists of a sample and hold buffer, an analog multiplexer, and sequencing logic. The sequencing logic generates sample clock and multiplexer select signals for each channel based on a counter which keeps track of which channel is to be connected

with the output. The TDM circuit was designed to send 8 CMUT signals with center frequency of 7 MHz 80% bandwidth via single cable. the clock frequency of the multiplexer needs to be 156.8 MHz or higher to satisfy the Nyquist sampling requirement. If the clock frequency is set to 200 MHz then the sampling frequency for each channel, will be 25 MSPS. The sampled analog signal pulses need to reach steady state fast enough so that the external ADC can sample the amplitude correctly. The multiplexer circuit can be programmed operate in link training mode and signal multiplexing mode. A key part of the DDD is the synchronization required between the TDM multiplexer and the sampler of the ADC. Before multiplexing the CMUT signals link training needs to be performed to synchronize the ADC with TDM. During the link training period transducer side electronics generate a proper training sequence. In the training sequence, channel 1 is connected to a fixed value voltage level V_{DC1} while other channels are connected to another value voltage level V_{DC2}. Figure 5.3 shows the configuration of the TDM during link training. By analyzing the TDM data during link training, it is possible to identify from the external ADC side which is channel 1 and properly phase align the TDM and ADC clock as there will be significant difference between one sample than the others.

During link training the multiplexer generates a pattern where the code for channel 1 is significantly different than the other channels as shown in Figure 5.3. The pattern is then sent out via buffer through the μ-coax cable to the external ADC. The phase of the ADC clock is then adjusted compared to the TDM clock. By analyzing the TDM data on the ADC side it is possible to identify which is channel 1 as there will be significant difference between one samples than the others. Once the channel 1 has been identified, the phase of TDM clock can be adjusted for optimum alignment between ADC and the TDM. The optimal alignment shall take place when only sample of channel 1 shall have one value and all others sample shall have different same value. As shown in Fig 5.3 when the relative phase difference of TDM and

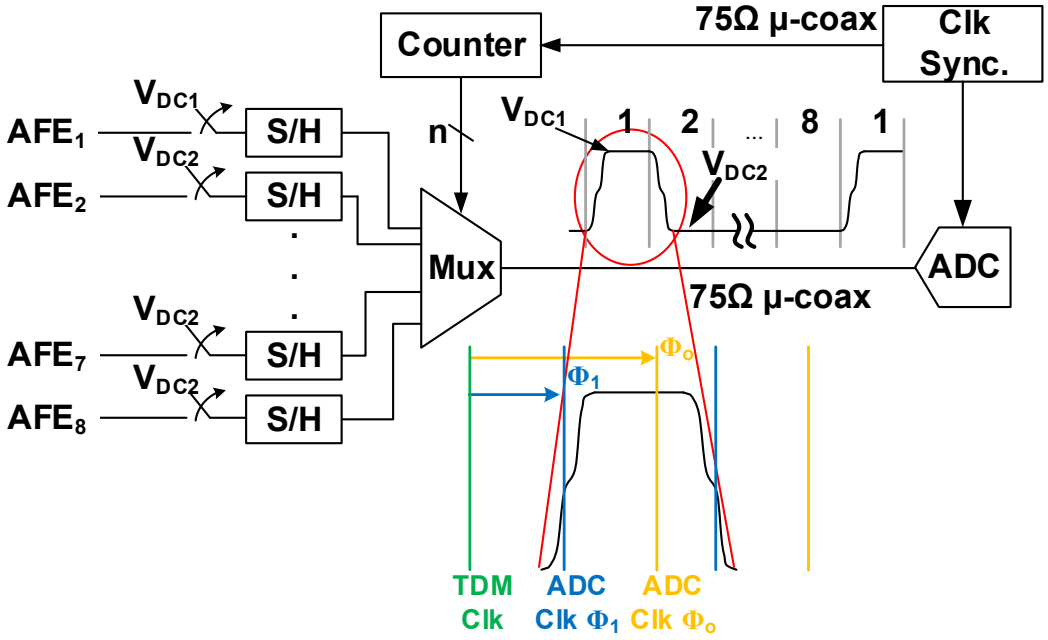

Figure 5.3: Link Training mode of the TDM circuit.

ADC clock is Φ_1 then not only channel 1 but also channel 2 shall have different value than rest of the channels. Now if the relative phase difference is Φ_o then only channel 1 shall have different value than the other channels and optimal phase alignment shall be achieved. The phase shift added to the ADC clock will then account for any propagation delays in the system, including the delay in the cables. Direct Digital Demutiplexed (DDD) technique allows the output data of the TDM directly to an ADC which will be running at same frequency as the TDM. By using a high-speed ADC which is capable of sampling at the same frequency as the TDM clock signal, the system can be designed such that each ADC sample corresponds exactly to one channel in the multiplexed data. This means that as the samples are taken, demultiplexing becomes a simple task of separating the data into groups consisting. of every n^{th} sample. This results in a data stream for each TDM channel which can each then be filtered and interpolated using DSP techniques. The detailed description

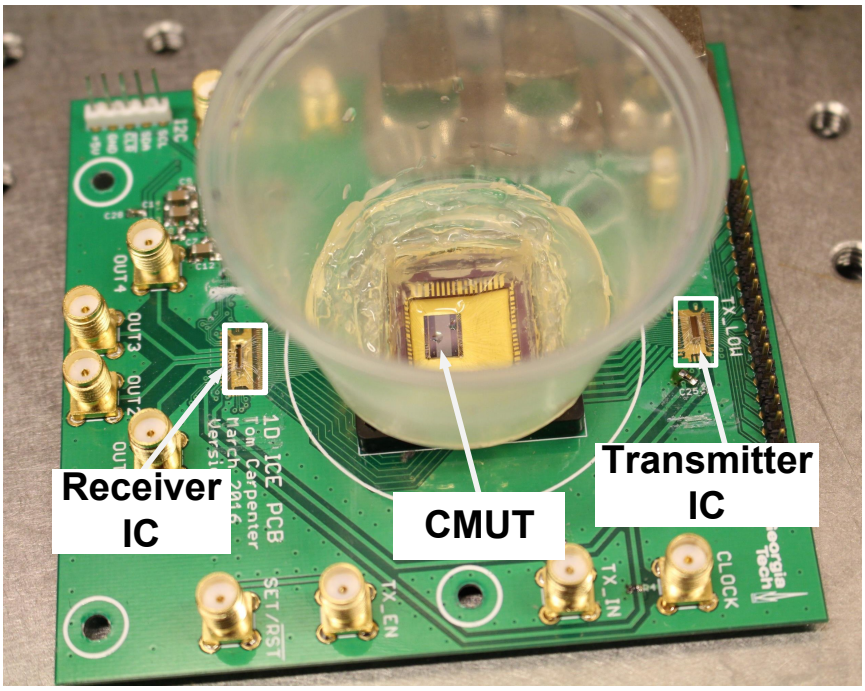

Figure 5.4: Fabricated PCB where the transmitter beamformer and receiver circuit with TDM were directly wireboned to the PCB and the CMUT was wirebonded to a 64-pin LCC package and placed inside a socket in the PCB.

of the multiplexing and DDD scheme has been reported in detail in [58].

5.2 Imaging Experimental Setup

To prove massive reduction of cable count is possible using both the proposed transmit beamformer and the TDM chip, the transmit beamformer and receiver ICs was wirebonded to a test PCB along with the 1-D CMUT transducer array. The same 1-D CMUT array shown in Figure 2.9 was used for the imaging experiment. Figure 5.4 shows the assembly of the fabricated PCB with transmitter beamformer and TDM receiver circuit. In the PCB SMA-type connectors were used to properly connect clock, data and TDM output signals of the ICs through the 1 meter length of 75Ω, 48 AWG μ-coax cable bundle to the FPGA and ADC. The same 200 MHz clock, data, power and control signals were routed via PCB to connect both the transmitter and the receiver circuit. The data cable which was used to program the transmitter

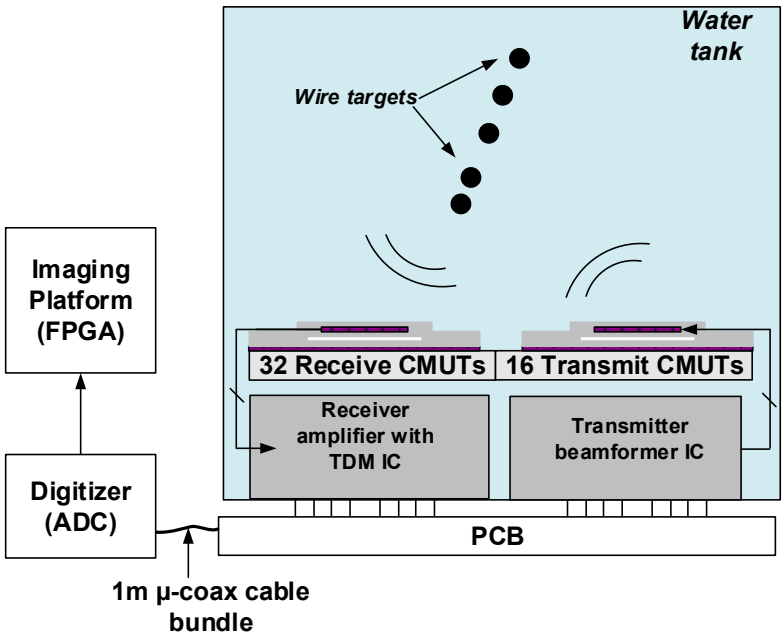

Figure 5.5: Imaging experiment test setup.

beamformer was used to control the 4 level TGC circuit of the receiver system. The CMUT was submerged in water and a 5-wire phantom target was being placed in the water tank. Figure 5.5 and Figure 5.6 shows detailed description of the experimental setup.

Figure 5.7 shows the proposed timing diagram of the overall imaging system test. The **Data_In** signal was used for programming the beamformer and during receive operation, a TGC control signal shall be sent through the same cable. When both **TX_En** and $\overline{\mathbf{R}}$ are low the entire system will be in reset mode. Once **TX_En** goes high the beamformer can be programmed and at the same time receiver link training can be done to phase align the ADC and TDM for direct digital demodulation. Once the beamformer is programmed and the ADC and TDM are properly aligned, then the $\overline{\mathbf{R}}$ signal can be de-asserted and the pulser shall transmit pulses according to the programmed delay and pulse width. Simultaneously the receiver electronics start processing the receive signal.

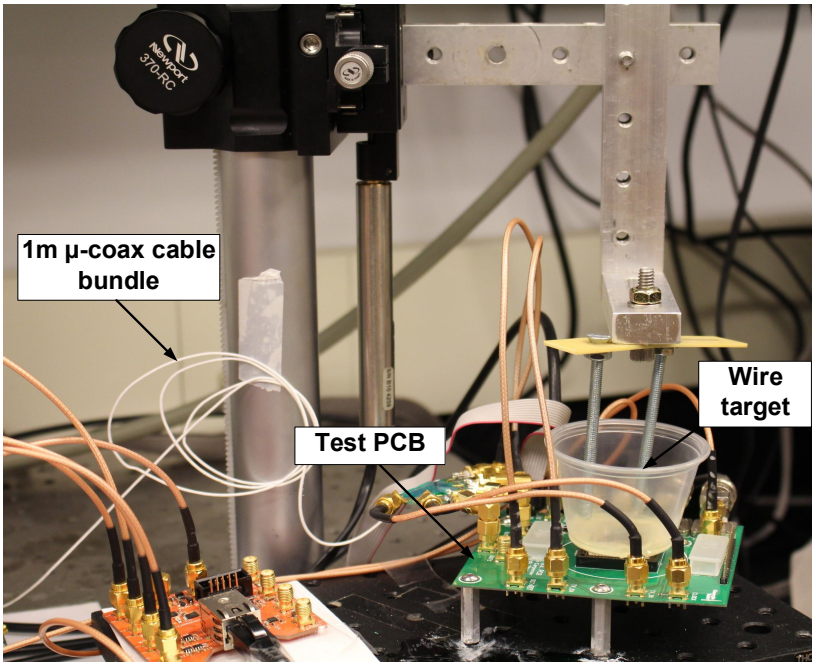

Figure 5.6: Photo of the experimental setup.

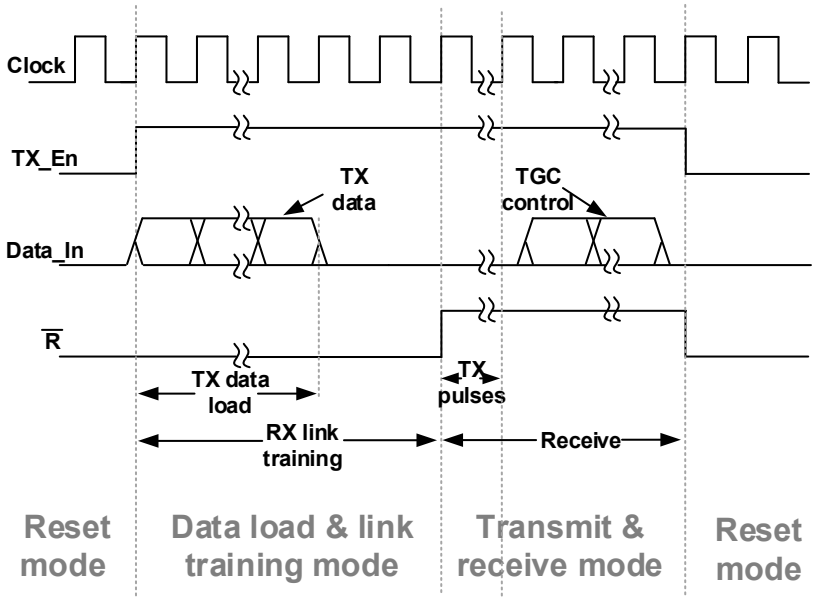

Figure 5.7: Timing diagram of the imaging system.

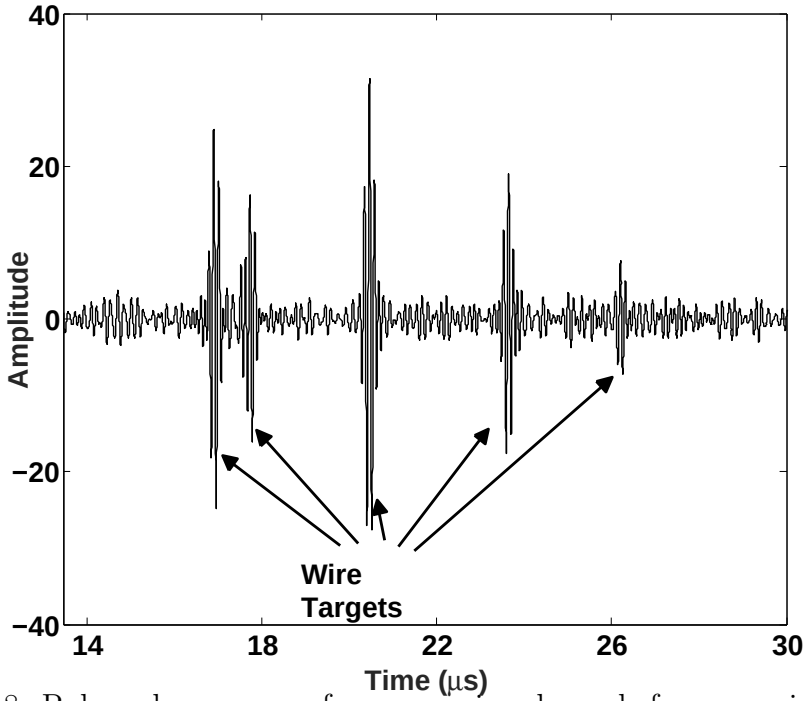

Figure 5.8: Pulse echo response from a receive channels from an wire targets.

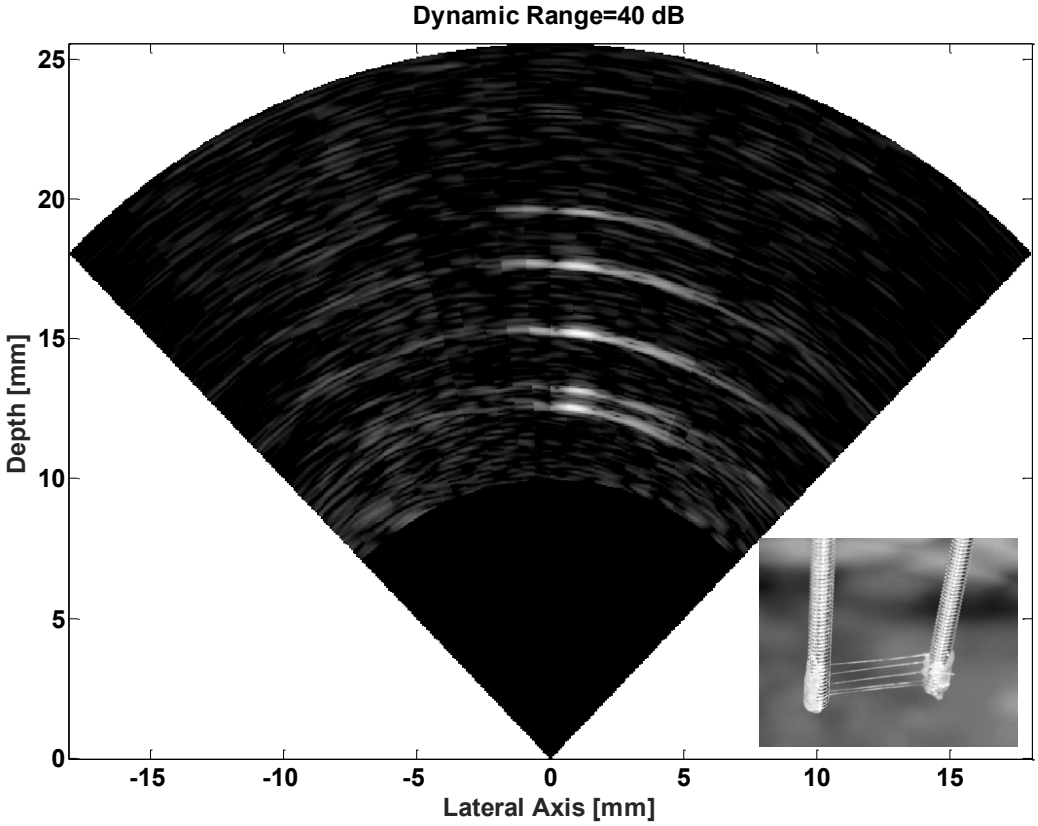

Figure 5.9: B-scan image of the wire phantom on yz plane obtained from the experiment. The dynamic range of the image is 40dB.

In this experimental setup using the TX beamformer, the programmed focused beam with a 65 ns pulse width was sent through the integrated high voltage pulsers connected to the CMUT transducer to generate a focused transmit beam. The receiver electronics connected to a further set of CMUT transducers were then used to capture echo signals from 5-wire phantom target placed above transducer array. The received signals then get multiplexed using the TDM circuity. The four TDM output signals from the IC are fed through 4 different 48 AWG μ-coax cables and a further external LNA stage (Texas Instruments LMH5401) which drives the input of a high-speed ADC (TI ADC16DX370) with 800 MHz analog bandwidth. The ADC is synchronized with a phase adjusted version of the 200 MHz clock fed to the both the transmitter and receiver ICs so that it can perform the direct digital demultiplexing (DDD) using the technique described in [58]. After performing the DDD, the digitized data were farther real time processed for phase correction and filtering in the Stratix V FPGA and then sent to a computer via PCI bus for image construction. Figure 5.9 shows the resulting image captured from the experiment.

CHAPTER 6
INTEGRATED SYSTEM

After the successful MPW shuttle run, a full wafer reticle was designed using 0.18 μm TowerJazz 60 V process. On the reticle, electronics for both 1-D and 2-D CMUT-on-CMOS array was designed. The receiver cable reduction technique was kept the same as MPW run. But to optimize power and area consumption, increase pulse voltage and add additional features like burst mode operation and pulse width controlled apodization the beamformer architecture was changed massively. To ensure proper data loading during programming the transmit beamformer and reduce number of cable, data can be encoded on the pulse width of the clock and sent out from the FPGA via single cable. To extract the data on the tip of the catheter, a PLL less simple decoding scheme is also introduced in this thesis. This thesis refers the designed beamformer in the full wafer run as beamformer-II. A test chip of the beamformer-II consisting of 32 pulsers was implemented in the full wafer run.

6.1 Transmit Beamformer Architecture II

To improve the performance of the beamformer circuit the transmit beamformer-II circuit is implemented in this thesis. This beamformer can generate 60 V pulses. Pulse-width of each pulses can be individually controlled. Also, the beamformer can be programmed to run in single pulse mode or Doppler mode. In Doppler mode number of pulses and pulse repetition frequency can be also programmed. A maximum of 8 pulses can be sent out from each firing in the Doppler mode. Instead of using separate cables for sending the clock and data to program the beamformer, in this version a data/clock decoding circuit is used to send data and clock on a single cable. The block diagram of the beamformer architecture II is shown in Figure 6.1.

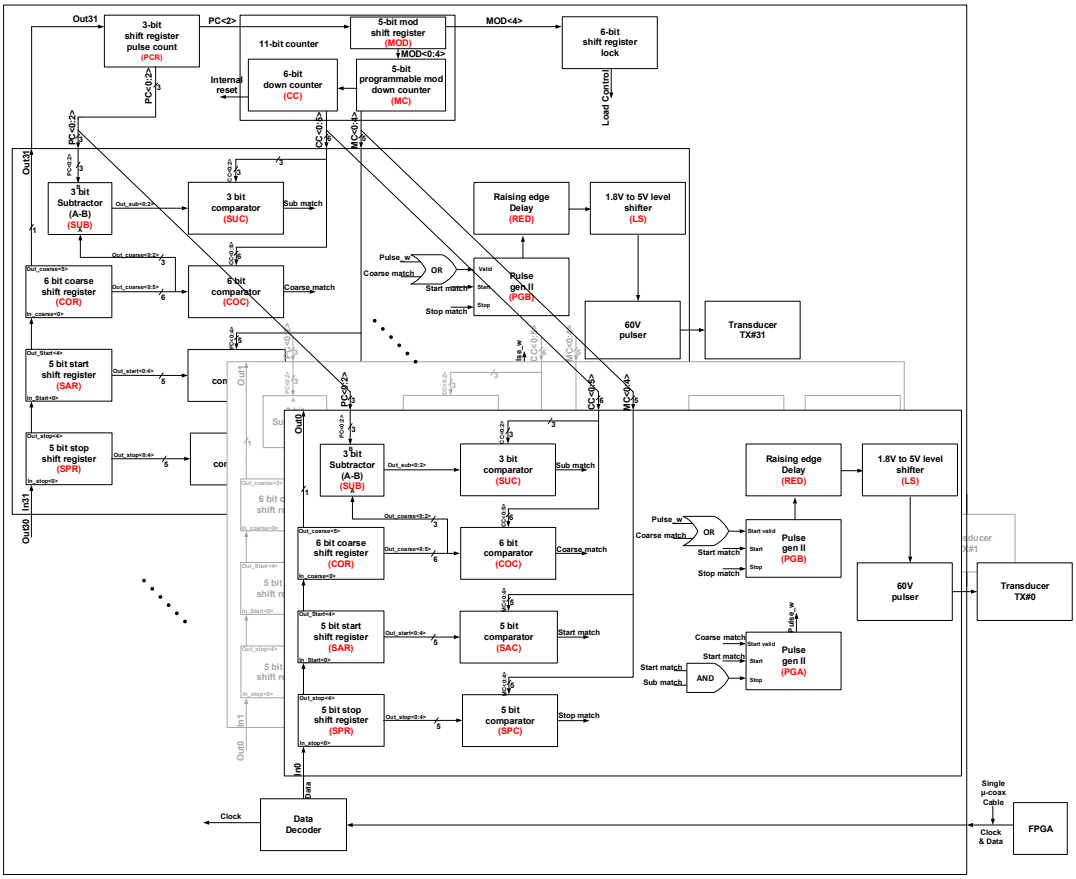

Figure 6.1: Block diagram of the implemented transmit beamformer architecture II.

The beamformer has a maximum delay of 10 μs and delay resolution of 5 ns. It consists an 11-bit global counter. The MSB 6-bits of the counter are fixed and starts counting form maximum value 111111_2 and mod of LSB 5-bit counter can be programmed to set the pulse repetition rate during Doppler mode operation. Each element consists 16-bit register to store delay and pulse width value for each pulser. The pulse width of each individual pulse can be varied independently which allows the option to distribute power to different transmit element in a programmed manner. Thus transmit apodization can be performed using the beamformer-II architecture by controlling pulse width of the transmit pulses on every channel [60, 61]. A 6-bit global shift register is used for controlling the data loading. A 3-bit global register is used to

store the total number of pulses fired from each transmitter and a subtractor is used in every element to keep track of how many pulses are fired during each transmission cycle. The beamformer-II can be programmed to fire only single pulse from each transmitter for normal transmit operation or can be programmed to fire up to 8 pulses during Doppler mode operation. The HV pulser designed for beamformer-II can be operated at 60 V and the voltage is limited by the process parameter. Unlike the HV pulser used in beamformer-I which uses a HV PMOS mirror to drive the output side HV PMOS, the HV pulser used in beamformer-II uses a resistor divider network and 5 V buffer driver that operates from 55 V to 60 V to drive a output side HV PMOS. Though this architecture uses additional 55 V from outside, the elimination of the PMOS mirror drastically reduces high current flowing through the pulser during the pulsing period and significantly reduces the size of the pulser as HV PMOS occupies significant area. Driving the HV PMOS with a 5 V buffer also increases the speed of operation of the pulser. As a result, smaller size HV PMOS can be used to drive the same load capacitance than before. Reducing the size HV PMOS reduces output parasitic capacitance as a result the size of output side NMOS can also be reduced. The area occupied by the 32 pulser beamformer-II IC is 2.88 mm^2 which is smaller size than 16 pulser beamformer-I, while having the capability to operate in single, Doppler and pulse apodization modes.

6.1.1 Data encoding and decoding

In previously reported literatures [32, 33, 48, 62, 63] the data and the clock were sent via separate cables to program the beamformer. Data and clock are synchronized from outside and are sent via different cables to the beamforming IC as shown in Figure 6.2(a). Due to mismatch in cable impedance or temperature the delay on the cables can be different. The synchronization between the data and clock can be disrupted due to mismatch in the cable delay and the programming of the beamformer

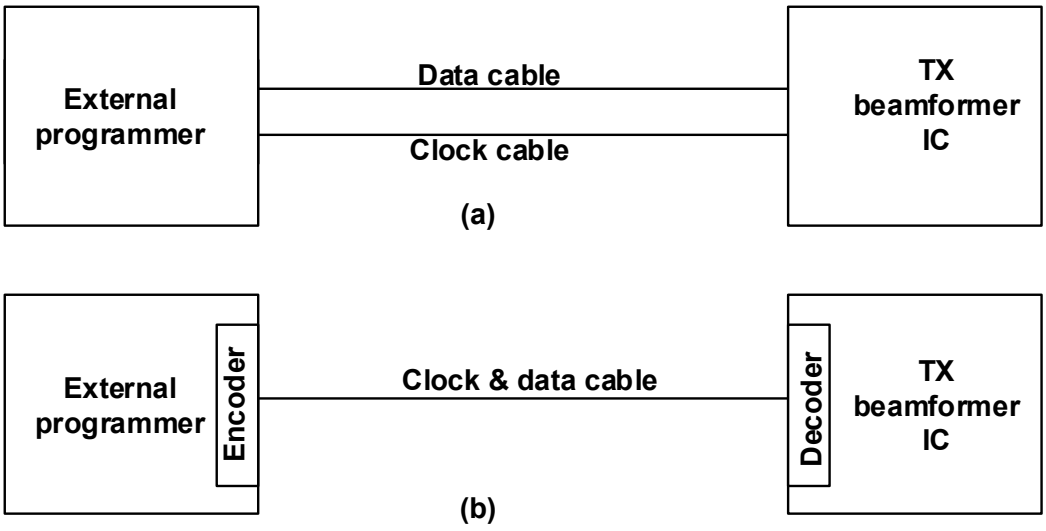

Figure 6.2: (a) Conventional separate cable (b) implemented single cable solution for data and clock for transmitter beamformer programming.

can get corrupted. One way this issue can be resolved is by encoding the data and clock together and send them via single cable as shown in Figure 6.2(b). Also encoding data on clock and sending them via single cable reduces the cable count.

There are various data encoding methods like Manchester, RZ, NRZ, AMI etc. But decoding the data and clock requires complex Clock Data Recovery (CDR) circuits. The CDR circuits consists Phase Lock Loops (PLL) which consumes significant power and area. Also it needs to lock with the incoming signal before decoding the clock and data. For ICE application, implementing a high speed PLL is extremely challenging on the tip of the catheter. On the other hand, if the data is encoded in the pulse width of the clock then it is possible to decode the data from clock without using complex CDR circuits. The data encoding method is shown in Figure 6.3. The repetition rate of the rising edge of the clock remains constant and duty cycle is changed according to the data. If the duty cycle is $> 50\%$ the data 1 is sent and if duty cycle is $< 50\%$ data 0 is sent. Since all the counter and other synchronous circuit are synchronized with the rising edge of the clock, the encode clock can be used directly as the clock

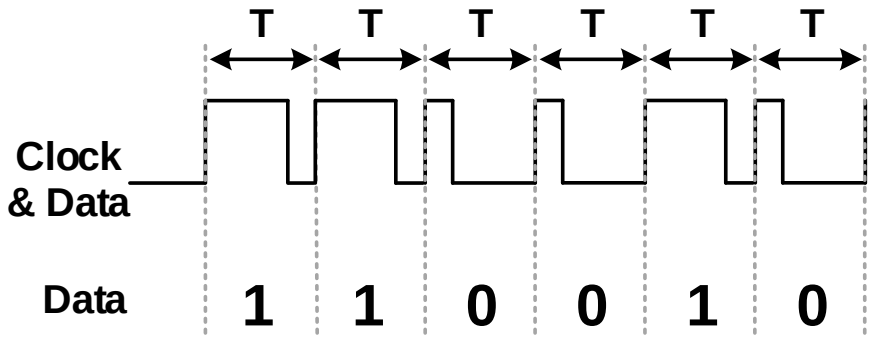

Figure 6.3: PWM data encoding.

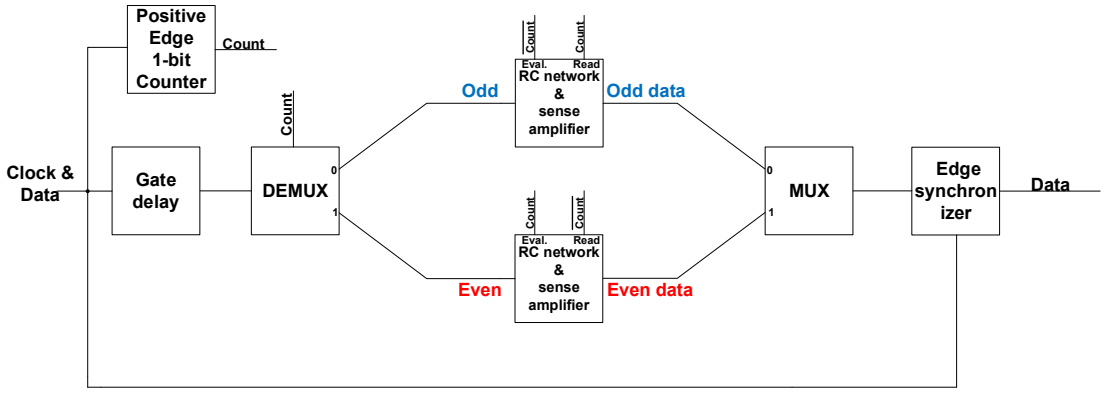

Figure 6.4: Block diagram of the data decoding circuit.

for the transmit beamformer circuit.

The encoded data can be extracted using sense amplifiers. Figure 6.4 shows the block diagram of the implemented PLL less data decoding circuit. The circuit consists a deserializer, two sense amplifiers with RC network and a serializer followed by a synchronizer circuit.

The functionality of the RC network with the sense amplifier is shown in Figure 6.5. Each sense amplifier with RC network requires two clock cycles to decode the data. During the first clock period, the capacitors C_1 and C_2 are charged (eval-

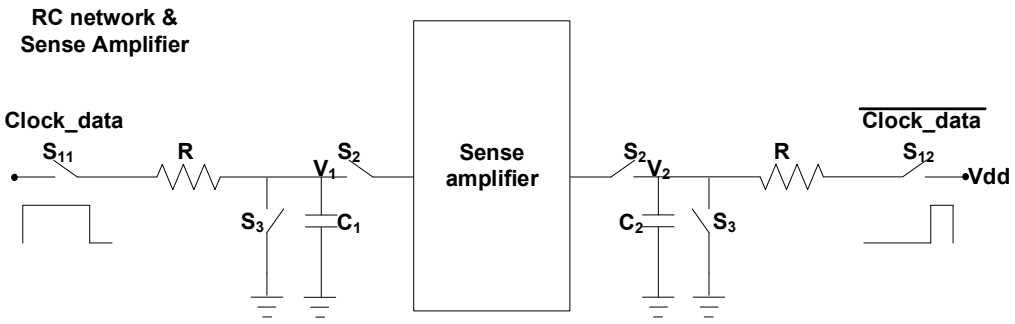

Figure 6.5: Data decoding with RC network a sense amplifier.

uation cycle). During the second clock period, the sense amplifier gives the decision based on the value of charged value of C_1 and C_2 (decision cycle).

During evaluation cycle switches S_2 remain off and switches S_{11} and S_{12} conduct. S_{11} and S_{12} gates are driven by the incoming Clock_data and its inverted signal respectively. Now if the Clock_data signal has a duty cycle $> 50\%$ then the capacitor C_1 will become more charged than C_2 and value of V_1 shall be greater than V_2. On the other hand,if the clock duty cycle in $< 50\%$ then V_2 stall be greater than V_1. During the decision period if $V_1 > V_2$ then the sense amplifier gives an output one and if $V_1 < V_2$ then the sense amplifier gives an output zero. Thus, in two cycle the RC network with sense amplifiers can decode the incoming Clock˙data signal. Since each block requires two clock cycles to decode a symbol, it is possible to use two sense amplifiers in parallel as shown in Figure 6.2 to decode the incoming signal so that in each clock period, a symbol can be decoded.

To verify the PLL less data decoding technique, a test decoder chip was implemented in 0.18 μm TowerJazz 1P4M 1.8 V process. Figure 6.6 shows the micrograph of the test circuit. The test IC was wire-bonded to a custom PCB to provide power and input signal. Clock and data were encoded from a FPGA and sent out via single 1-meter long μ-coax cable to the test decoder circuit.

The encoded data were probed with an active probe and captured with an os-

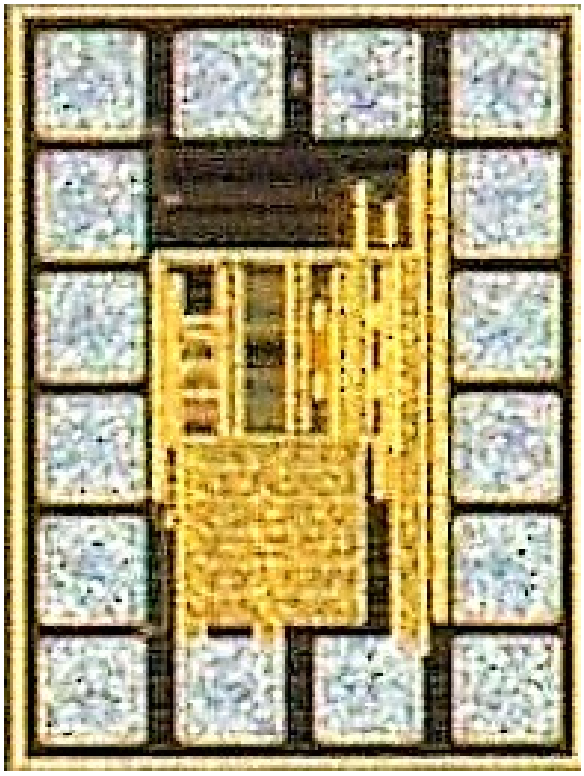

Figure 6.6: Micrograph of the test data decoding circuit.

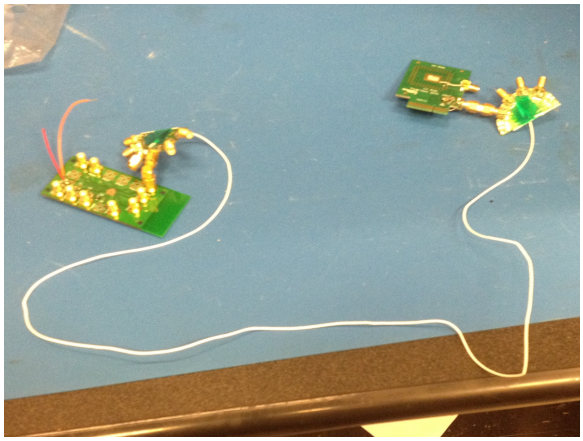

Figure 6.7: Test setup of the data decoding test circuit.

cilloscope. The output of the decoder was captured using the digital input of the oscilloscope.

From the input and output data, it can be seen that when the input duty cycle is $> 50\%$ the decoder output is 1 and when the input duty cycle $< 50\%$ the decoder output is 0. Also, there is a two-cycle latency between the input and output data of

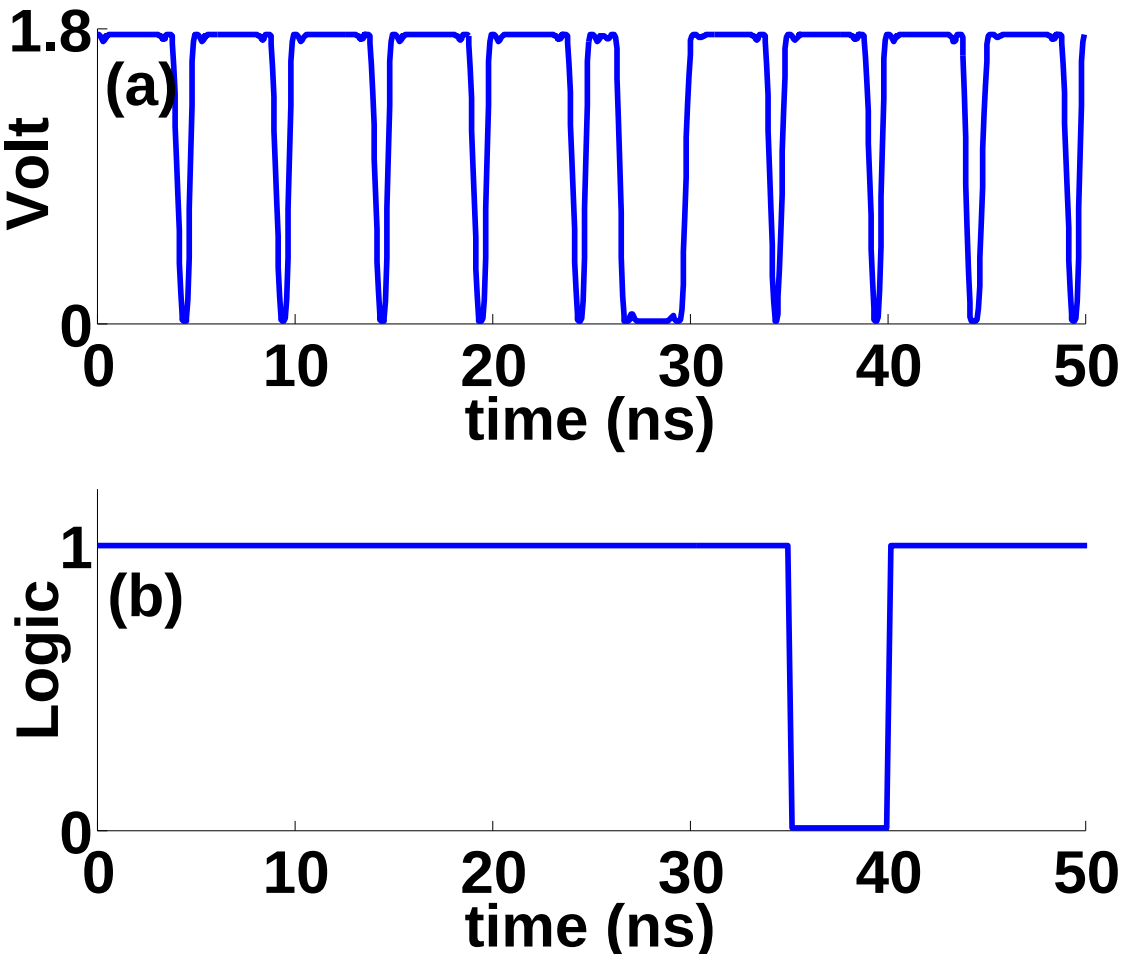

Figure 6.8: Captured (a) encoded input signal (b) decoded output signal.

the decoder.

6.1.2 60 V Transmit Pulser

One of the major changes performed in the beamformer-II architecture is the high voltage pulser. The HV pulser-I used for the beamformer-I has been reported in several recent applications. One major disadvantage of this pulser is that when the output pulse is on, the diode connected HV PMOS and associated NMOS stay on. As a result, high current flows through the inner branch, which can cause high IR drop in the chip. This can also affect the data stored the low voltage memory cells as the high current shall flow through the ground and can cause ground voltage to jump up on the chip. The high current can also damage the chip. The high current condition while the output of the pulser is high is illustrated in Figure 6.9. Though the Towerjazz HV process supports high voltage up to 60 V, to avoid high current through the IC while high voltage pulsers are on, the beamformer-I was operated at 30 Volt. Another issue of the HV pulser-I is pull up slew rate depends on the ratio of diode connected HV PMOS and the output stage PMOS. In order to achieve high pull up slew rate, the output PMOS needs to be large as it is driven by a diode connected PMOS.

To overcome these issues the pulser of beamformer-II has been modified as shown in Figure 6.10. Instead of using a diode connected HV PMOS to drive the output PMOS a resistor divider and 5 V buffer chain circuit which swings from 55 V to 60 V is used to drive the output PMOS. When the signal Inn set to low and Inp to high the M_2 closes and M_1 starts conducting. When M_1 is on the current through this branch gets limited by the resistor network and it allows a maximum current of 3 mA. During this time input of the 5 V buffer becomes 55 V. The signal passes through the buffer and turns on the output PMOS. In this pulser the PMOS gate signal travels via M_1, resistive network and then through the 5 V buffet circuit. So, the output PMOS gate signal is delayed compared to the output NMOS's gate signal. This helps reduction of transient power consumption when pulse goes high as the output stage

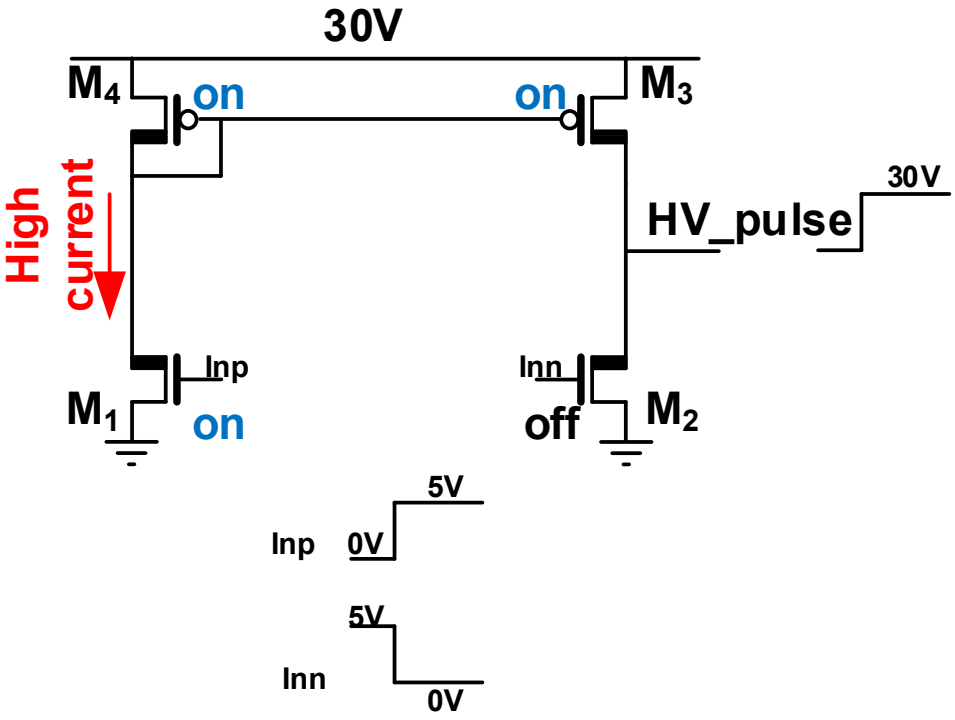

Figure 6.9: High current path of pulser-I circuit.

NMOS first turn off and then PMOS turns on. But when the pulse goes low this delay of PMOS gate signal via the pulser architecture can cause 60 V to be shorted to ground as NMOS can turn on before PMOS gets turned off. To avoid this kind of condition a rising edge delay is added to the path of Inn signal. The rising edge delay circuit add one clock cycle delay when the signal changes from low to high. This one clock cycle ensures that HV PMOS M_3 shall first turn off and the HV NMOS M_2 shall turn on.

6.1.3 Individual pulser cell logic

Each pulser cell consists of a 5-bit shift register (SPR) to store the delay value of falling edge and 5-bit shift register (SAR) to store the delay value of rising edge of the pulse. Also, each pulser consists a 6-bit shift register (COR) to store the coarse delay of the pulse. A 3-bit subtractor circuit (SUB) is added to each pulse

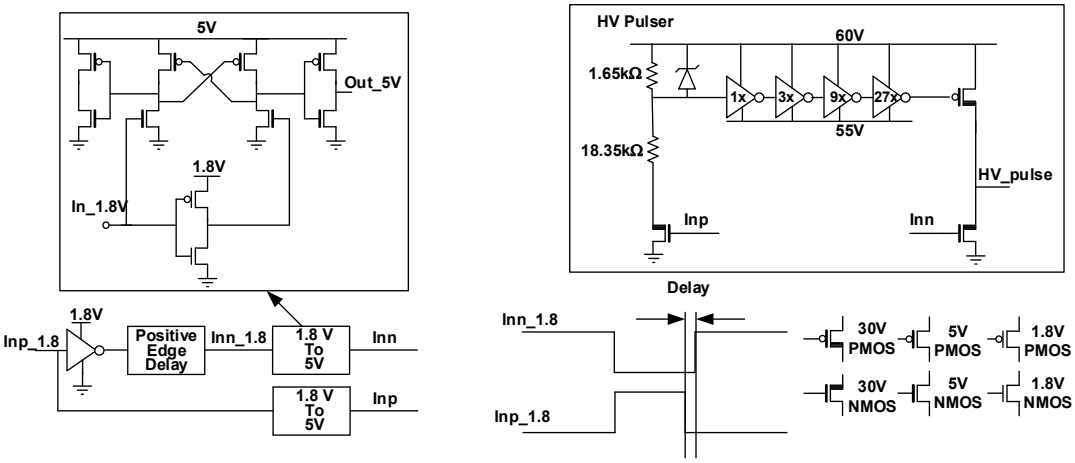

Figure 6.10: Circuit diagram of pulser-II circuit.

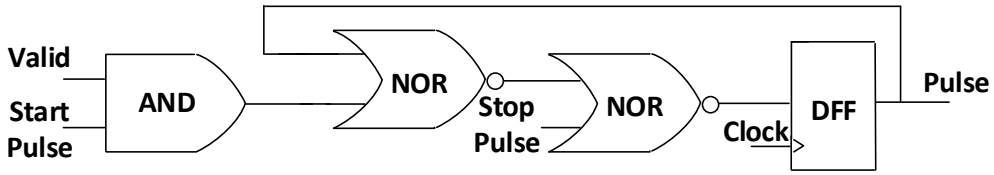

Figure 6.11: Circuit diagram of pulse generator logic circuit.

to keep count of pulse transmitted during Doppler mode. Each pulser also consists two 5-bit comparator (SPC) and (SAC) to compare the value of 5-bit start and stop registers with the value of mod counter, a 6-bit comparator (COC) to compare the value of coarse register to coarse counter and a 3-bit comparator (SUC) to compare the subtracted value of LSB 3-bit of the coarse register to the value stored in the global 3-bit pulse count register. There are AND, OR and two low voltage pulse generator circuit (PGA) and (PGB) implemented in each cell of this beamformer. The implemented pulse generator circuit is shown in Figure 6.11.

To ensure safe and low power operation of the 60 V pulser circuit, a rising edge delay (RDG) is implemented in each pulser cell. The circuit diagram of the rising edge delay is shown in Figure 6.12. The output of rising edge delay (RDG) drives

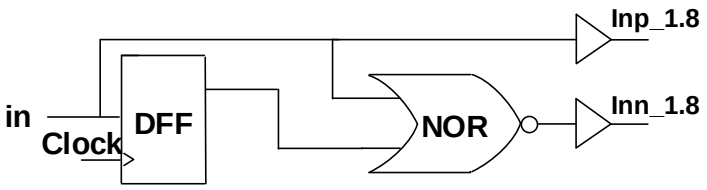

Figure 6.12: Circuit diagram of the rising edge delay circuit.

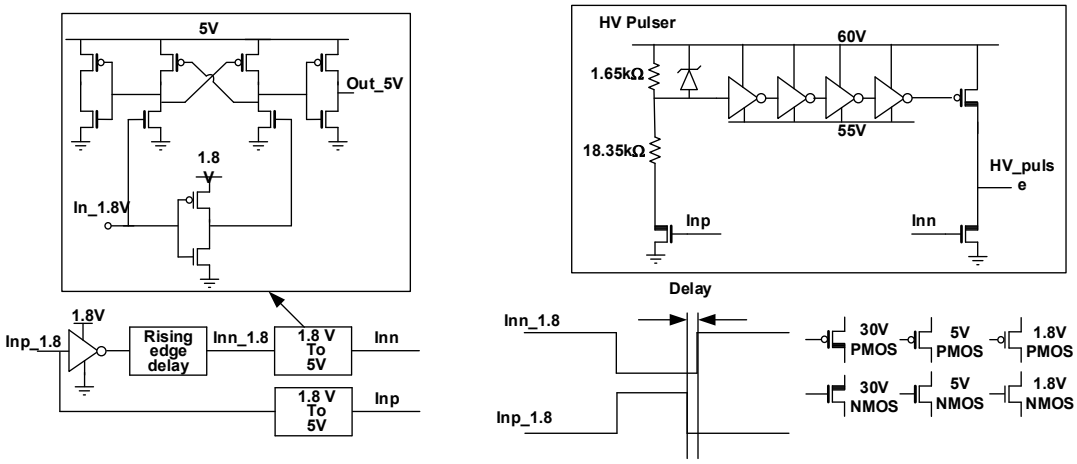

Figure 6.13: Circuit diagram of 60 V pulser circuit.

the 60 V pulser circuit. The circuit diagram of the new 60 V pulser is shown in Figure 6.13.

6.1.4 Programming Beamformer-II

This beamformer requires only one external signals $\overline{\mathbf{R}}$ to control the programming and firing cycle of the beamformer. Before programming the beamformer, all the register and counters are cleared by de-asserting the external $\overline{\mathbf{R}}$ signal low. After resetting the registers and the counters, the $\overline{\mathbf{R}}$ signal is set high and the programming data is sent from the FPGA via a μ-coax cable through the Data_In pin of the Transmit beamformer.

For programming the 32 TX pulser beamformer each programming cycle a 526-bit

$(32 \times 16 + 3 + 5 + 6 = 526)$ long data packet needs to be sent to program the entire beamformer. The first 6 bits of the data packet are used as preamble bits 111111_2, and when they reach the 6-bit lock registers, the output of the AND6 becomes high and data is stopped. This then triggers the counter and registers to be programmed with appropriate value. After data has been loaded the internal 11-bit counter starts counting. As shown in Figure 6.1 the MSB 6-bits coarse counter (CC) are used for coarse match and LSB 5-bits of the mod counter (MC) are used for fine match of the delay and set the pulse width of each pulser. The mod counter starts counting 11111_2 to the programmed mod value. Once mod counter reaches programmed mod value it goes back to 11111_2 and starts counting again. The coarse counter starts from 111111_2 and for each cycle of the mod count the value of the coarse counter decreases by 1_2. Once the value of the coarse counter reaches 000000_2 an internal reset signal is sent to all the delay, lock and mod registers and mod counter is set to the value 11111_2 . In the next clock cycle the coarse counter reaches 111111_2 and coarse counter is held on this value. The internal reset signal gets de-asserted and new set of data to program the beamformer can be sent from FPGA. To program this beamformer the external $\overline{\mathbf{R}}$ signal doesn't need to be de-asserted to low to reset the registers to load new data set. Once data is loaded properly the counters start counting and when the coarse counter value reaches 000000_2 the internal reset signal is generated. To stop the transmit beamformer from the FPGA the $\overline{\mathbf{R}}$ signal can be set to low. The programmable 5-bit mod counter is used to have control over the pulse repetition rate during Doppler mode. The block diagram of each pulser cell is shown in Figure 6.14.

6.1.5 Single pulse mode operation

During single pulse mode operation, the value of the 3-bit pulse count register PCR and mod register MOD are programmed to 000_2 and 00000_2 respectively so each

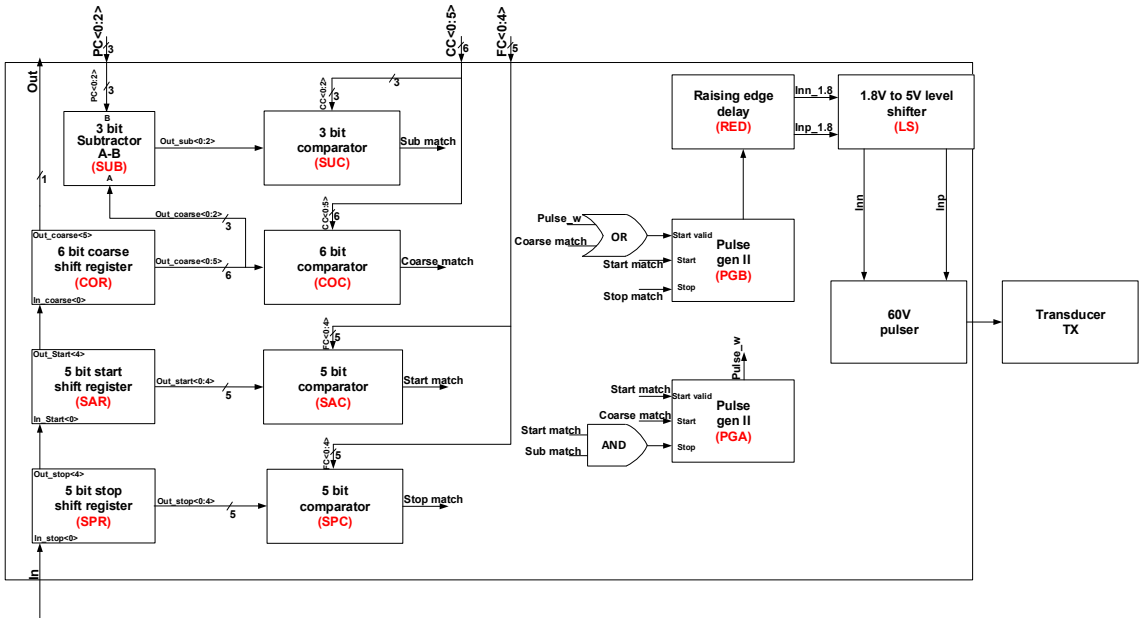

Figure 6.14: Block diagram of each pulse cell.

pulser is pulsed only once. The delay value of each pulser element is loaded from the FPGA. After loading the data to the beamformer the 11-bit CC and MC counter starts counting from 11111111111_2. For any individual pulser When the value of the coarse counter CC$< 0 : 5 >$ matches the value of the COR register the Coarse match signal becomes high. Since PCR value is set to 000_2 in the single pulse mod the Sub match signal also becomes high. Now when MC counter value matches the value of SAR the Start match signal becomes high also. During this time both the Start valid, Star and Stop inputs of PGA are high. Since Start and Stop signals are high at the same time the output of PGA Pulse_w remains low due to the implemented logic of Pulse gen II circuit. On the other hand, for PGB only Start valid and Star input signal are now high and output of PGB becomes high and pulse starts. Finally, when the value of MC matches the value of SPR register then the Stop input of PGB becomes high and the pulse stops. Thus, start delay of each pulse can be set by programming the value of the COR and SAC register. On the other hand, the pulse width of each individual pulse can be adjusted by the programming the value of SPR

compare to SAR.

As an example, if pulser 1 requires delay of 1 μs and pulse-width of 45 ns and pulser 2 requires delay of 2 μs and pulse-width of 55 ns, then the COR register of pulser 1 is set to 111001_2, SAR and SPR value is set to 10111_2 and 01110_2 respectively. On the other hand, the COR, SAR and SPR of pulser 2 are programmed to 110011_2, 01111_2 and 00100_2 respectively. As mentioned earlier once data load completes the CC and MC counter starts counting from value 111111_2 and 11111_2 respectively. After 1 μs the CC value reaches 111001_2 and MC value reaches 10111_2 and matches with the stored value of COR and SAR of pulse 1. Output of pulser 1 goes high. After another 45 ns, the value of MC reaches 01110_2 and matches the value of SPR of pulser 1. Output pulse then goes low. The CC and MC counter value reaches value 110011_2, 01111_2 after 2 μs and matches the value of COR and SAR register of pulser 2 and output of the pulser goes high. After 55 ns MC counter reaches 00100_2 and matches the value of SPR and pulser output goes low.

In the above-mentioned example, the CC value remains constant during the entire period while pulse is high. Now delay and pulse width may be chosen in such a way that CC value changes during when pulse is high. For example, if delay of pulser 1 was chosen to be 750 ns and pulse width 45 ns then COR, SAR and SPR register value will needed to be set to 111011_2, 00111_2 and 11110_2. Now when CC reaches 111011_2 and MC reaches 00111_2 the pulser 1 starts pulsing. Now in order to reach the value of 11110_2 MC needs to cross over 00000_2 which will cause CC to change value to 111010_2. Once pulse starts, the change in CC doesn't affect the pulse output as the logic of pulse generator is such that coarse match is only required only to start a pulse. Once a pulse starts only a pulse at the stop pin stops the pulse. In this design, different element can have different pulse width as they each has its own start and stop register. The delay and pulse width can be adjusted with one clock period resolution. The maximum pulse width generated by this beamformer can be as long

as 32 clock period long.

6.1.6 Doppler mode operation

During Doppler mode operation, the value of the global PCR register sets equal to the number of burst pulses. For example, if two pulses is required PCR value is set to 010_2 and if eight pulses is required then PCR is set to 111_2. The pulse repetition rate is set by the programmed value of the MOD register which sets the mod of the MC counter. For example, if the pulse repetition rate in Doppler mode is desired to be 120 ns then MOD register is set to 00111_2.

Like single pulse mode in Doppler mode initial delay of pulses are stored in the COR and SAR registers and pulse width of each pulse is determined by the value difference of the SAR and SPR registers.

As mentioned earlier in Doppler mode the PCR value is set to the desired pulse number that would require to be fired. The PCR value is subtracted from the LSB 3-bits of the COR register and compared with the LSB 3-bits of CC$< 0 : 2 >$. When CC$< 0 : 2 >$ value reaches the value equal to (COR$< 0 : 2 >$-PCR$< 0 : 2 >$) then the output of the SUC comparator goes high.

After loading the data to the beamformer the 11-bit CC and MC counter starts counting from 11111111111_2. In Doppler mode, the MC counter reaches its mod value and then goes back to value 11111_2 and then count down again. In every cycle of the MC counter, the value of the CC counter decreases by 1_2. When the value of CC becomes equal to the value of COR then Coarse match signal becomes high and when value of MC becomes equal to value of the (SAC) the Start match signal becomes high. For Doppler mode PCR value is greater than 000_2, so Sub match signal shall remain low. As a result, output of PGA Pulse_w signal becomes high. Pulse_w signal remains high until both Start match and Sub match becomes high together. As long the Pulse_w signal is high for every pair of Start match and Stop

match a pulse would be generated. While the Coarse match remain high only for one MC counter cycle. The LSB 3-bits CC counter reaches the value equal to value stored in SUB once MC counter goes through the number of cycles equal to the value stored in PCR register. Once the LSB 3-bits CC matches the value of SUB, the Sub match signal goes high. During this period when MC value becomes equal to the SAR the Stop signal of PGA becomes high and Pulse_w signal goes low. Since both Coarse match and Pulse_w are low, no new pulses are generated by the PGB. Thus, the number of pulse is controlled by the value stored in PCR and pulse repetition rate is controlled by the value stored in MOD register. For the first pulse, the Pulse_w signal becomes high after the Coarse match and Start match signal high. To ensure the first pulse is not missed Pulse_w signal and Coarse match signals are combined via 2 input OR gate to drive the start valid input signal of PGB. As an example, if in Doppler mode, pulser 1 requires having an initial delay of 1 μs and then have 8 burst pulses with pulse width of 60 ns and pulses are repeated every 120 ns. Then the value of global PRC and MOD register is set to 111_2 and 00111_2 respectively. The value of the COR SAR and SPR value needs to be set to 110111_2, 10111_2 and 01011_2 respectively. After data loading the 11-bit counter starts counting. When the value of CC becomes 110111_2 the Coarse match signal becomes high and remains high for the one mod counter cycle. During this cycle when MC becomes equal to 10111_2, the Pulse_w becomes high and remains high until COR becomes 110000_2 and MC again becomes equal to 10111_2. In other words, Pulse_w remains high for 8 cycles of the MOD counter as MOD register was set to 111_2. Now anytime when Coarse match or Pulse_w is high when MC matches the value of SAR output of PGB will go high and when MC matches the value of SPR the PGB value will go low. During the 8 cycle of MC counter when the Pulse_w or Coarse match remains high there shall be 8 times the MC value shall match the value of SAR and SPR. This shall generate 8 pulses. Also since the MOD register is programmed to 00111_2 the cycle time for each MC

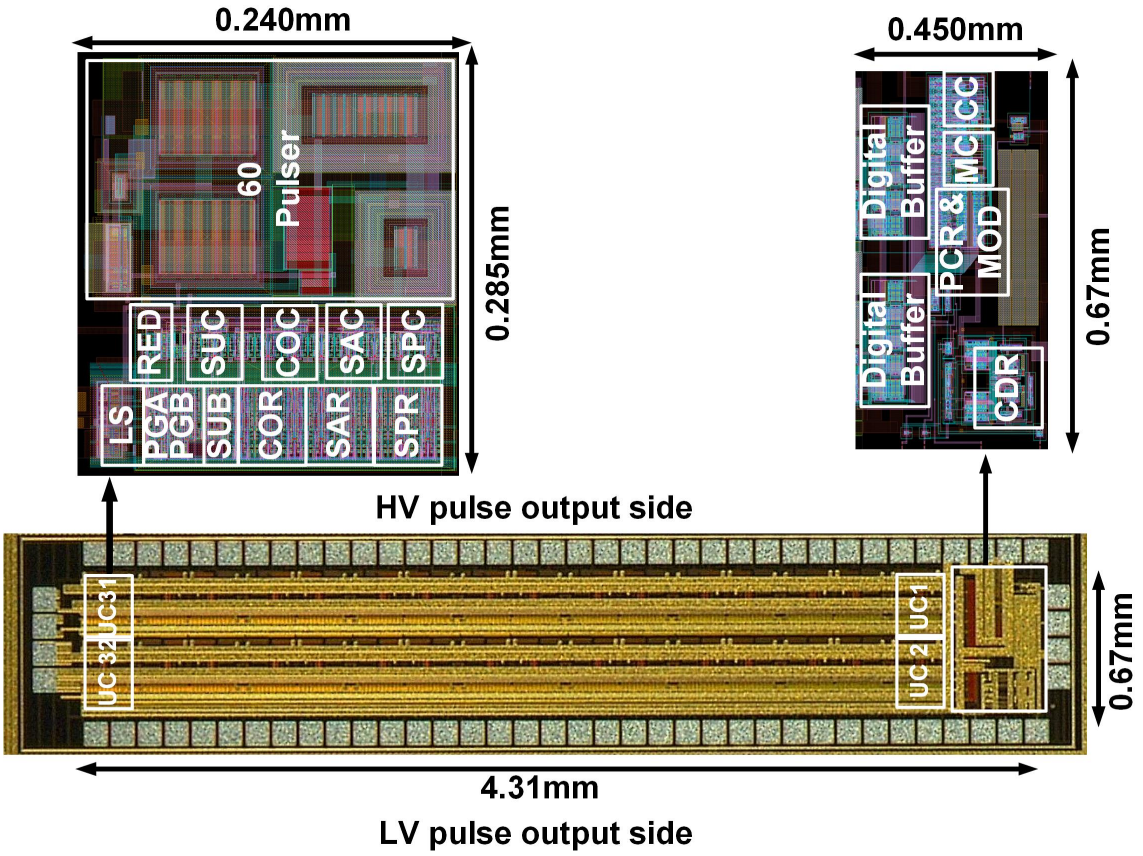

Figure 6.15: Micrograph of the 32 pulser Beamformer II IC with detailed floor plan. Area 4.31 mm × 0.67 mm.

counter shall be 120 ns which set the pulse repetition rate. Like single pulse mode, in Doppler mode the pulse width of each pulser can be adjusted independently by programming the value of SPR compared to SAR.

6.1.7 Beamformer II Characterization Experiment

A prototype of the Beamformer II with 32 channel beamformer-IC was designed in 0.18 μm TowerJazz 1P4M HV process and occupies a 4.31 mm × 0.67 mm area (without the bond pads). Figure 6.15 shows the micrograph of the fabricated beamformer-II IC with detailed floor plan.

The fabricated beamformer-II IC was diced and wire bonded to a PCB to properly power and connect the clock and control signals to the circuit. The beamformer-II

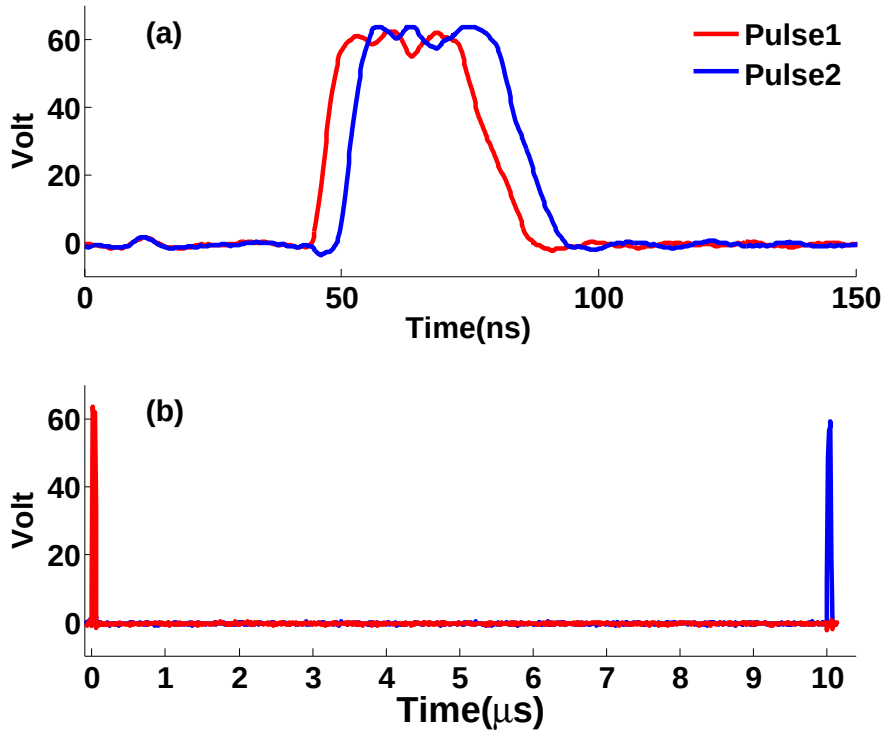

Figure 6.16: (a) Minimum delay between two pulses 5 ns (b) Maximum delay of 10 μs.

was programmed with FPGA. Delay resolution and rise and fall time was measured. measured rise time was 5.4 ns and fall time was 11.4 ns only when one transmitter was activated and was connected to a 15 pF load. The beamformer was programmed to generate minimum and maximum delay between two pulses and the delays were measured. Figure 6.16 the measured minimum and maximum delay that can be generated by the beamformer.

The beamformer was programmed to generate Doppler pulses. Figure 6.17 shows 4 and 8 pulses generated for Doppler mode operation.

The beamformer was also programmed to verify the individual pulse width control capability. Figure 6.18 shows individual pulse width control of two different pulses during single firing.

A monolithically integrated 32 TX and 32 RX imaging system was designed for 1-D CMUT array in the wafer run reticle. Figure 6.19 and 6.20 shows micrograph of the prototype system with voltage amplifier and transimpedance amplifier as front-end

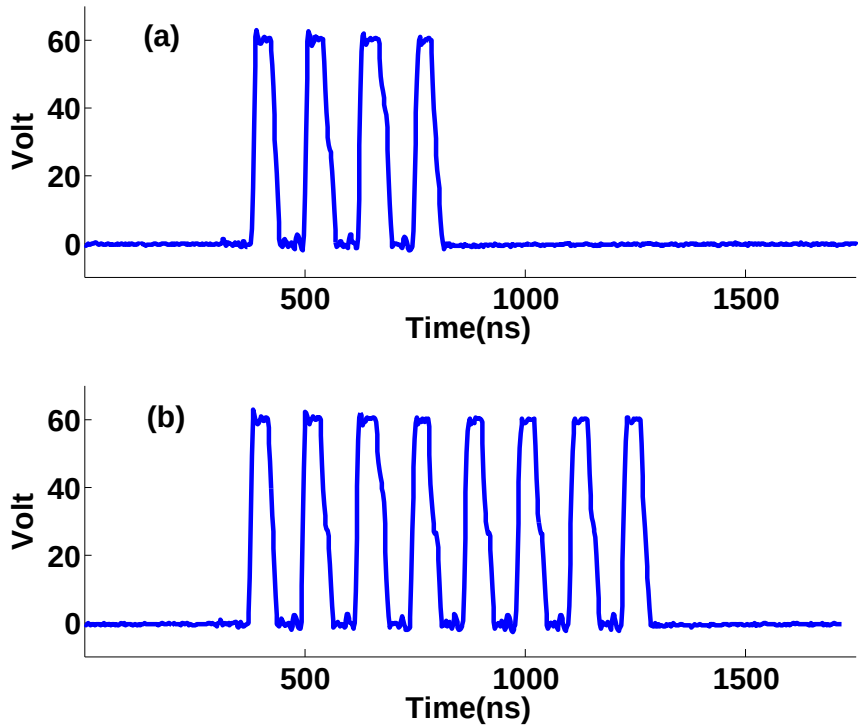

Figure 6.17: (a) 4 Doppler pulses (b) 8 Doppler pulses.

amplifier respectively.

Along with the prototype systems, electronics for 2-D array was also designed in the full wafer run. Electronics array for both Vernier array and cross array were designed. The Figure 6.21 shows the micrograph of the designed electronics for CMUT-on-CMOS Vernier array and a zoomed picture of each pixel of the array. The TX and RX electronics shall use separate CMUT element. The designed array consists 165 pixels where 160 of the pixel consists 2 TX element and 1 RX element. 5 pixels consists only TX elements. A total of 330 TX and 160 RX are implemented in the array. There are 10 TDM circuit to multiplex the output data from 80 RX channels at a time. To get data from the entire 160 receivers 2 TX firing are required. During the first firing the odd RX elements are connected to the high speed TDM circuit in the second firing even RX elements are connected. Thus, only using 2 TX firing data from all 160 RX gets collected. The 330 TX and 160 RX element Vernier array only requires 20 cables for programming the transmit beamformer and collecting the data

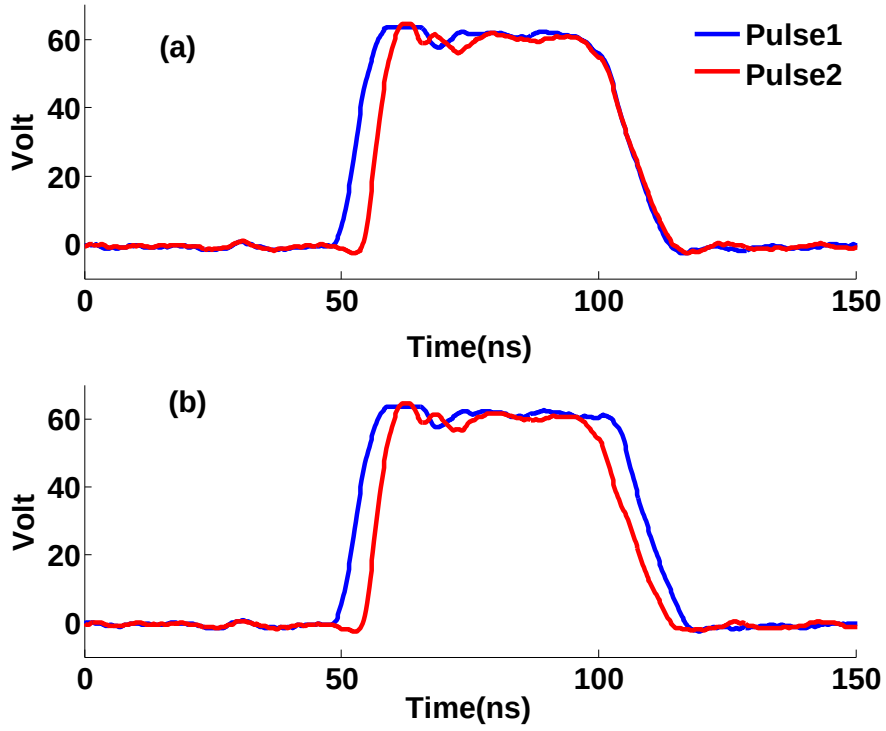

Figure 6.18: Pulse width is varied by using different (a) start value (b) start and stop value.

Table 6.1: CABLE DISTRIBUTION OF THE VERNIER ARRAY

Purpose	**Cable Count**
Receiver Multiplexed Signal	8
Power (1.8 V, 5 V, 55 V, 60 V, Analog GND, Digital GND and HV GND)	7
Clock and Data	2 (LVDS)
Reset Signal	1
External Bias	1
CMUT Bias	2
Total	20

from TDM circuits. The cable distribution of the Vernier array is given in Table 6.1

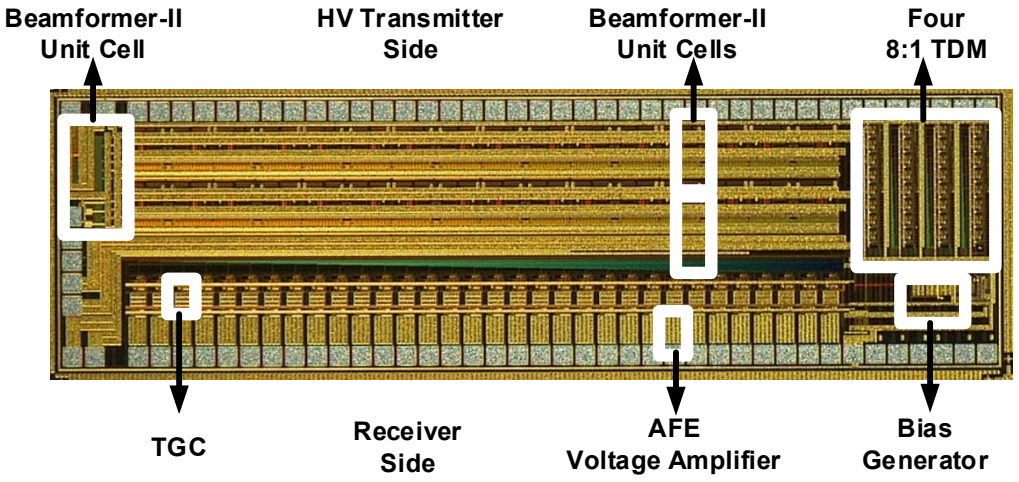

Figure 6.19: Micrograph of the Micrograph of 32 TX and 32 RX with voltage amplifier and beamformer-II ICE prototype system. Area 5.02 mm $\times$ 1.22 mm.

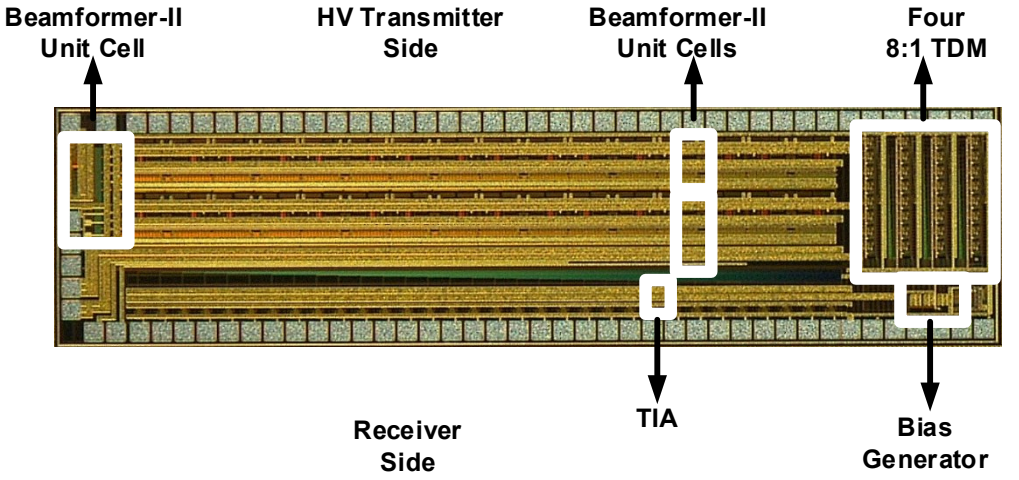

Figure 6.20: Micrograph of 32 TX and 32 RX with transimpedance amplifier and beamformer-II ICE prototype system. Area 5.02 mm $\times$ 1.03 mm.

It can be seen from Figure 6.21 that almost entire silicon space has been occupied with CMOS electronics and no more empty space is left. Good care was taken to optimize the layout of the electronics. The HV PMOS and HV NMOS occupied significant area. If one can use more advanced technology node with smaller HV

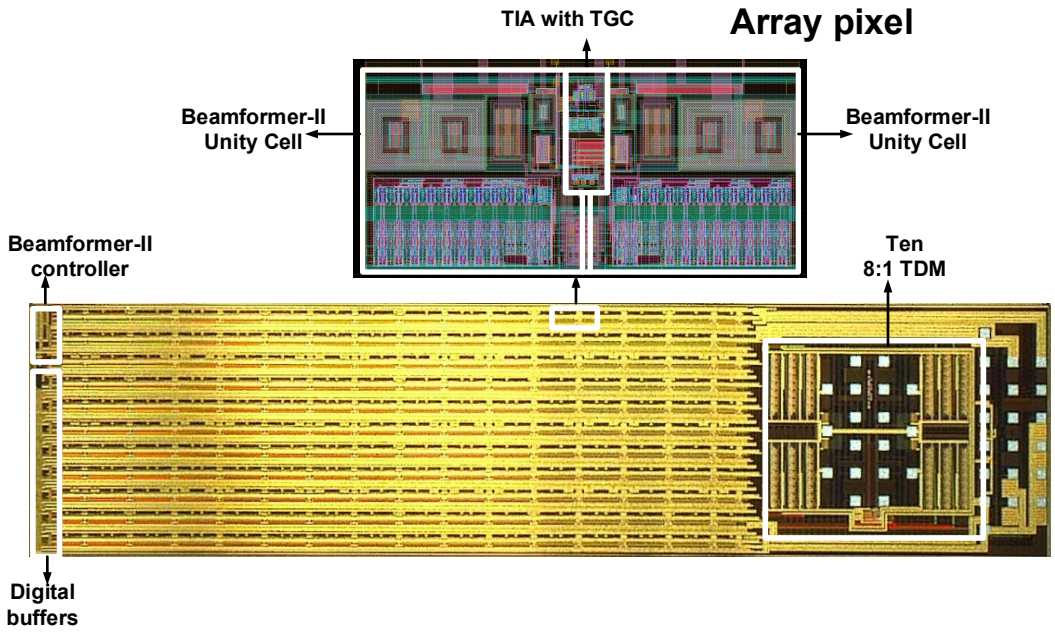

Figure 6.21: Micrograph of the designed Vernier array. Size 10.9 mm × 2.7 mm.

PMOS and HV NMOS which has similar drive strength then one can increase the number of element count. Also for 64 element linear array, the size of the electronics can be much smaller than the transducer array.

CHAPTER 7
CONCLUSION AND FUTURE WORK

This thesis shows that it is possible to implement electronics that fit at the tip of a catheter for cable reduction for both the transmitter and receiver subsystems in an intracardiac echocardiography imaging system.

While exploring the receiver cable reduction technique, this thesis first tried to implement Orthogonal Frequency Division Multiplexing (OFDM). An 8×1 OFDM circuit was designed in 0.35 μm 2P4M TSMC process and operates from a 3.3 V supply. The chip consists of a low noise trans-impedance amplifier, single to differential converter, anti-aliasing filter, frequency up-converter mixer, band-pass filters, combiner, differential to single ended converter and high frequency buffer line driver. Post layout simulation results were presented in [64]. The IC was fabricated and building blocks were tested. The electrical results of the capacitive feedback TIA and anti-aliasing filters are reported in Chapter 3 of this thesis. Though the post layout results were promising but the bandpass filter bank was found to be unstable as it is very challenging to design 8^{th} order gm-C bandpass filters with sufficient phase margin within the power and area restrictions. These filters are extremely sensitive to silicon process variations and would require a tuning mechanism for each individual filter to nullify the effect of process variation. This can be achieved at the cost of additional power, area or external cables. Therefore, this solution is not suitable for high density ICE array where area, power and cables are extremely limited.

The thesis then explores Time Division Multiplexing (TDM) technique for cable reduction, which appears to be more feasible solution for ICE application. The thesis shows implementation of Direct Digital Demodulation (DDD) of the TDM signals. Utilizing DDD allows TDM output to be fed to an ADC which is running at the

same frequency of the TDM signal. DDD eliminates the need for high frequency ADC, which need to run at least twice the speed of TDM, or the need for analog switches, filters and a number of low frequency ADCs that are required in standard TDM demultiplexing chain. As a result, less amount of data needs to be processed in the real-time imaging system, which help the overall system speed. A prototype TDM multiplexer stage for 8 input channels, has been fabricated in 0.35 μm 2P4M TSMC process and operates from a 3.3 V supply. The IC doesn't have any analog front end low noise amplifier. Instead, the input stage consists unity gain buffer. The objective of designing the prototype IC was to verify TDM with Direct Digital Demodulation and determine crosstalk between the channels as a result of multiplexing. The output of the IC was connected to a 1m length of 48AWG μ-coax cable with 0.17 mm outer diameter, which can be used in a catheter application to an ADC which was operated at same frequency as the TDM circuit (200 MHz). The fabricated IC was fully characterized and results were published in [58].

While TDM coupled with DDD looks promising for cable reduction in the receiver side of the front-end is not particularly advantageous unless transmit beamformer electronics with small area are also integrated at the catheter tip while connected to the outside system with a reduced number of cables. This thesis also demonstrates successful design and implementation two different programmable beamformer architectures, which can be placed on the tip of the catheter. The beamformer-I consists of 16 pulser and has a maximum delay of 1.27 μs. It also consists 2 on-chip 8-bit global down counters. One counter starts from the maximum value and the other start counting down from a programmed value. Each pulser consists 8-bit registers to store delay value for each pulse. Each pulser must share a common pulse width that can be varied with 5 ns resolution. The maximum voltage the beamformer-I could be operated was 30 V, limited by the high current that passed through the high voltage pulser during pulsing without damaging the chip. Beamformer-I archi-

tecture does not allow multi pulse doppler mode operation. One single pulse can be sent out from each pulser during one transmission cycle. The total area occupied by the 16 pulser beamformer-I was 2.9 mm^2. The beamformer requires different cables for clock and data to program the beamformer from an external FPGA. The delay mismatch between the cables can cause wrong data to be loaded during programming the beamformer. The beamformer-I was designed in 0.18 μm TowerJazz 60 V process in a MPW shuttle run.

A 32 element receiver electronic was designed in the same MPW shuttle run. The receiver IC design includes a Low Noise Amplifier, Time-Gain Compensation (TGC) coupled with analog Time Division Multiplexing (TDM) circuitry to achieve an 8:1 cable reduction. The RX IC operates from the same 1.8 V supply as the digital logics of beamformer-I. Post layout simulation results of the receiver electronics was reported in [56]. An imaging system was designed by wire-bonding the fabricated IC to a test PCB along with a 1D CMUT transducer array. The CMUT was placed in a water tank. Using the beamformer, the programmed focused beam with a 65 ns pulse width was sent through the integrated high voltage pulsers connected to the CMUT transducer to generate a focused transmit beam. The receiver electronics connected to a further set of CMUT transducer elements were then used to capture echo signals from an air-water interface, then multiplex the signals using the TDM circuit. The Signal to Noise Ratio (SNR) was calculated for each channel to measure the uniformity of the receive channels by comparing the RMS power of the received echo pulse with the RMS noise power from a quiet part of the received signal. A brief description of the imaging system was reported in [62]. Each block of the receiver chain was also experimentally verified. A 5-wire phantom target was being placed in the water tank. Focused beam was sent out from the HV beamformer-I to scan the entire image space. The pulse echo for each transmit pulse was multiplexed and sent out via μ-coax cable to the image processing system by the receiver chain.

The detailed description of the beamformer-I and receiver circuit along with imaging results were reported in [63].

A imaging system with the 32 channel TDM receiver and 16 channel transmitter beamformer-I was successfully designed from the MPW shuttle run. In order to optimize overall area of the MPW die, discrete transmitter and receiver circuits were designed. After the successful completion of the shuttle run a complete integrated system with 330 transmit element and 160 receiver elements was designed in a full wafer run. The system requires only 21 cables. Two firings are required to collect data from all receiver elements. Area and power optimized beamformer-II was developed and implemented in the full wafer run. This thesis also introduces true single cable programmable transmit beamformer by introducing a data encoding over the clock pulse width and removing the need for an additional cable to send the data. The data can be easily decoded form clock without the need of any PLL circuit. Eliminating the need for PLL makes the system simpler as ICE system is turned on and off at 10% duty cycle mode, and a PLL would need to lock to the incoming data every time the system is powered on.

It can be seen from 2-D array electronics that almost the entire silicon space under the array has been occupied with CMOS electronics and no more empty space is left to put more electronics to increase array density. More advanced process node may be required to increase the element count. Increasing the transmit element number will not add any cable because the required data to program the beamformer can be sent by just varying the pulse width of the clock. But if only 8×1 TDM is used for reducing the receive channel cable count then for every 8 receiver elements one more cable would be required. To reduce receiver channel cable count further, one can use a μ-beamforming [43] technique to combine 9 channels first. One advantage of using μ-beamforming is that the beamformed signals bandwidth remains the same as the receiver channels. After the μ-beamformer a high roll-off anti-aliasing filter can be

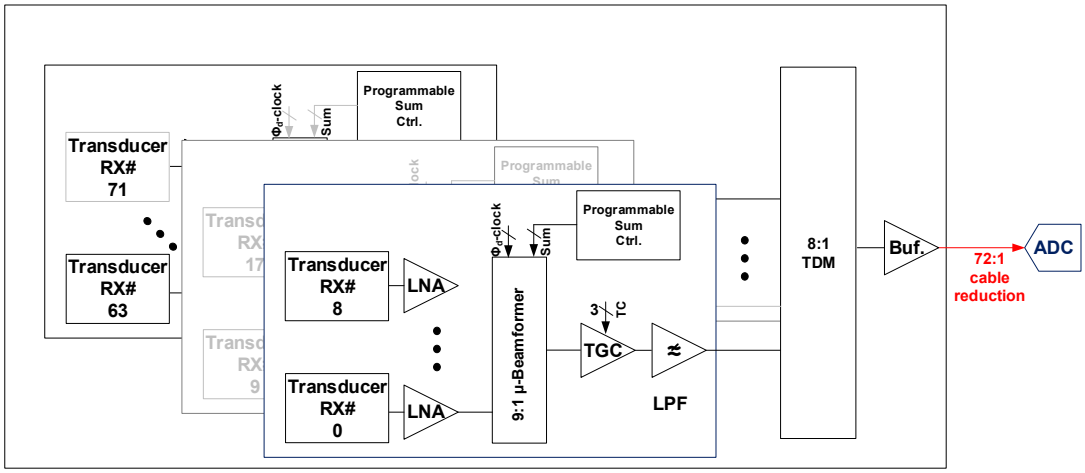

Figure 7.1: Block diagram of receiver architecture combining 9×1 μ-beamformer and 8×1 TDM to send out 72 receiver element data via single cable.

placed to eliminate any high frequency component generated by the μ-beamformer. Performing 8×1 TDM to the beamformed received channels, the cable count can be reduced to 72×1. Figure 7.1 shows the conceptual block diagram of how the μ-beamformer and TDM can be combined together to reduce receiver cable count.

In summary, this thesis demonstrated the feasibility of cable reduction for ICE catheters and opened the path for practical large element count 3-D imaging ICE catheters.

Appendices

APPENDIX A
EXPERIMENTAL EQUIPMENT

In this work we restrict our focus in developing cable reduction technique for ultrasound imaging system. Time-division multiplexing coupled with direct digital demultiplexing along with programmable transmit beamformer provides an alternative reduction strategy which is well suited to the requirements of CMUT on CMOS based ultrasound catheters. The development of a complete CMUT on CMOS based imaging system is beyond the scope of the propose work. The cable reduction techniques shall be validated by wirebonding CMUT imaging array with the designed CMOS chips. To complete the research work, active CMUT arrays was fabricated by Dr. Degertekin′s MIST group. Other facilities such as high speed TI ADC16DX370EVM board, Onda Hydrophones HGL 0085, Newport Motion Controller and Stratix V FPGA are available in Dr. Degertekin′s lab.

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